BURR - BROWN®

PCM1702P
PCM1702U

BiCMOS Advanced Sign Magnitude 20-Bit DIGITAL-TO-ANALOG CONVERTER

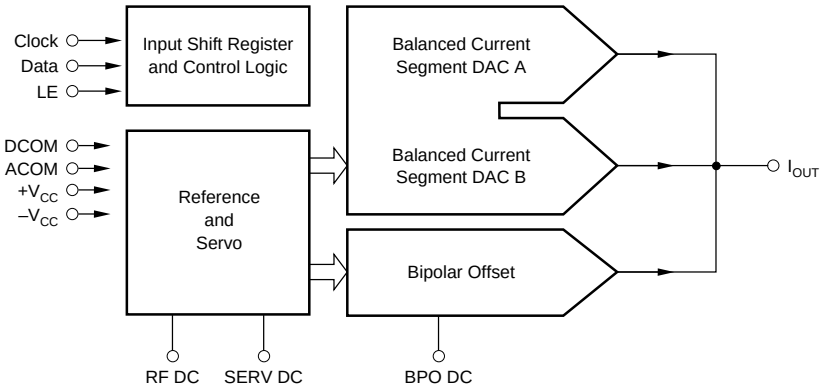
FEATURES

- **ULTRA LOW –96dB max THD+N (No External Adjustment Required)**
- **NEAR-IDEAL LOW LEVEL OPERATION**
- **GLITCH-FREE OUTPUT**
- **120dB SNR TYP (A-Weight Method)**
- **INDUSTRY STD SERIAL INPUT FORMAT**
- **FAST (200ns) CURRENT OUTPUT (±1.2mA)**
- **CAPABLE OF 16X OVERSAMPLING**
- **COMPLETE WITH REFERENCE**
- **LOW POWER (150mW typ)**

DESCRIPTION

The PCM1702 is a precision 20-bit digital-to-analog converter with ultra-low distortion (–96dB typ with a full scale output). Incorporated into the PCM1702 is an advanced sign magnitude architecture that eliminates unwanted glitches and other nonlinearities around bipolar zero. The PCM1702 also features a very low noise (120dB typ SNR: A-weighted method) and fast settling current output (200ns typ, 1.2mA step) which is capable of 16X oversampling rates.

Applications include very low distortion frequency synthesis and high-end consumer and professional digital audio applications.



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PDS-1175B
Printed in U.S.A. June, 1995

SPECIFICATIONS

All specifications at 25°C, $\pm V_{CC}$ and $+V_{DD}$ = ±5V unless otherwise noted.

PARAMETER	CONDITIONS	PCM1702P/U, -J, -K MIN	TYP	MAX	UNITS
RESOLUTION		20			Bits
DYNAMIC RANGE, THD + N at –60dB Referred to Full Scale, with A-weight			110		dB
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}		+2.4		$+V_{DD}$	V
V_{IL}		0		0.8	V
I_{IH}	$V_{IH} = +V_{DD}$			±10	µA
I_{IL}	V_{IL} = 0V			±10	µA
Data Format			Serial, MSB First, BTC[1]		
Input Clock Frequency			12.5	20.0	MHz
TOTAL HARMONIC DISTORTION + N[2]					
P/U V_O = 0dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–92	–88	dB
V_O = –20dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–82	–74	dB
V_O = –60dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–46	–40	dB
P/U, -J V_O = 0dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–96	–92	dB
V_O = –20dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–83	–76	dB
V_O = –60dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–48	–42	dB
P/U, -K V_O = 0dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–100	–96	dB
V_O = –20dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–84	–80	dB
V_O = –60dB	f_S = 352.8kHz[3], f = 1002Hz[4]		–50	–44	dB
ACCURACY					
Level Linearity	At –90dB Signal Level		±0.5		dB
Gain Error			±0.5	±3	%
Bipolar Zero Error[5]			±0.25		%
Gain Drift	0°C to 70°C		±25		ppm of FSR/°C
Bipolar Zero Drift	0°C to 70°C		±5		ppm of FSR/°C
Warm-up Time			1		minute
IDLE CHANNEL SNR[6]	Bipolar Zero, A-weighted Filter	110	120		dB
ANALOG OUTPUT					
Output Range			±1.2		mA
Output Impedance			1.0		kΩ
Settling Time	(±0.003% of FSR, 1.2mA Step)		200		ns
Glitch Energy			No Glitch Around Zero		
POWER SUPPLY REQUIREMENTS					
Supply Voltage Range: $+V_{CC} = +V_{DD}$		+4.75	+5.00	+5.25	V
$-V_{CC} = -V_{DD}$		–4.75	–5.00	–5.25	V
Combined Supply Current: $+I_{CC}$	$+V_{CC} = +V_{DD} = +5V$		+5.00	+9.0	mA
Combined Supply Current: $-I_{CC}$	$-V_{CC} = -V_{DD} = -5V$		–25.00	–41.0	mA
Power Dissipation	$\pm V_{CC} = \pm V_{DD} = \pm 5V$		150	250	mW
TEMPERATURE RANGE					
Operating		–25		+85	°C
Storage		–55		+125	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$) / $Signal_{RMS}$. (3) D/A converter sample frequency (8 x 44.1kHz; 8x oversampling). (4) D/A converter output frequency (signal level). (5) Offset error at bipolar zero. (6) Measured using an OPA627 and 5kΩ feedback and an A-weighted filter.

ABSOLUTE MAXIMUM RATINGS (DIP Package)

Power Supply Voltage	±6.5VDC
Input Logic Voltage	DGND—0.3V~+V_{DD}+0.3V
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Power Dissipation	500mW
Lead Temperature (soldering, 10s)	260°C

ABSOLUTE MAXIMUM RATINGS (SOP Package)

Power Supply Voltage	±6.5VDC
Input Logic Voltage	DGND—0.3V~+V_{DD}+0.3V
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Power Dissipation	300mW
Lead Temperature (soldering, 5s)	260°C

PIN ASSIGNMENTS (DIP Package)

PIN	MNEMONIC	PIN	MNEMONIC
1	DATA	9	+V_{CC}
2	CLOCK	10	BPO DC
3	+V_{DD}	11	I_{OUT}
4	DCOM	12	ACOM
5	–V_{DD}	13	ACOM
6	LE	14	SERV DC
7	NC	15	REF DC
8	NC	16	–V_{CC}

PIN ASSIGNMENTS (SOP Package)

PIN	MNEMONIC	PIN	MNEMONIC
1	DATA	11	+V_{CC}
2	CLOCK	12	BPO DC
3	NC	13	NC
4	+V_{DD}	14	I_{OUT}
5	DCOM	15	ACOM
6	–V_{DD}	16	ACOM
7	LE	17	SERV DC
8	NC	18	NC
9	NC	19	RFE DC
10	NC	20	–V_{CC}

PACKAGE INFORMATION[1]

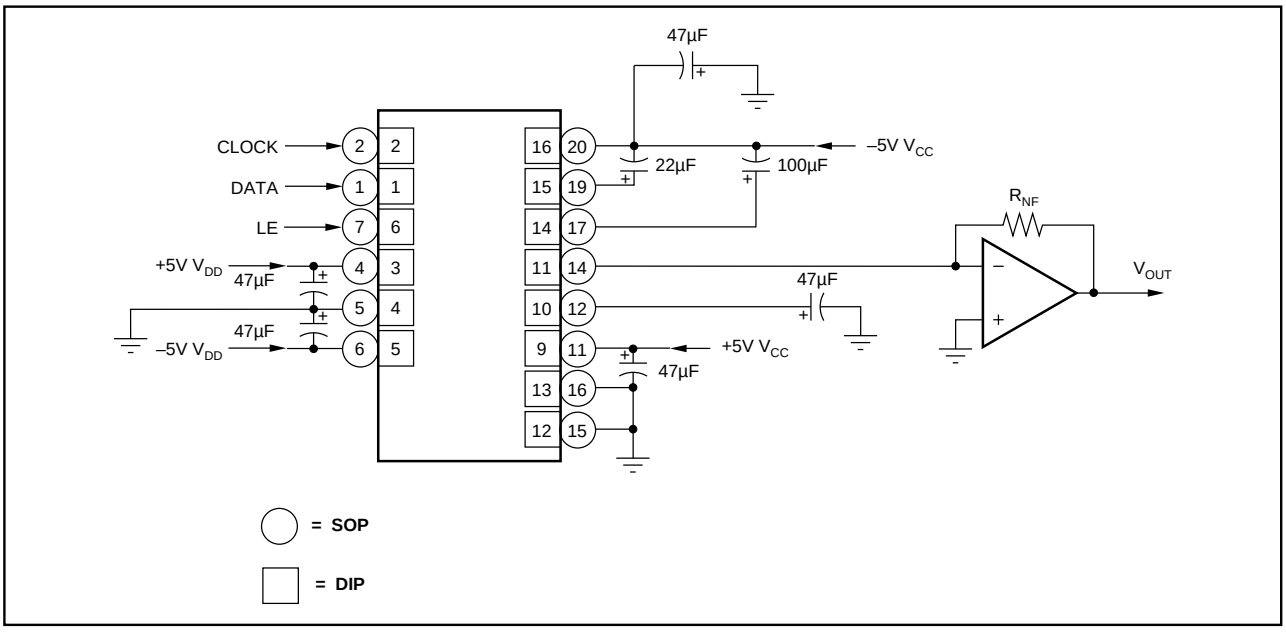
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM1702P	16-Pin Plastic DIP	180
PCM1702U	20-Pin Plastic SOP	248

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

GRADE MARKING (SOP Package)

MODEL	PACKAGE
PCM1702U	Marked PCM1702.
PCM1702U-J	Marked with white dot by pin 10.
PCM1702U-K	Marked with red dot by pin 10.

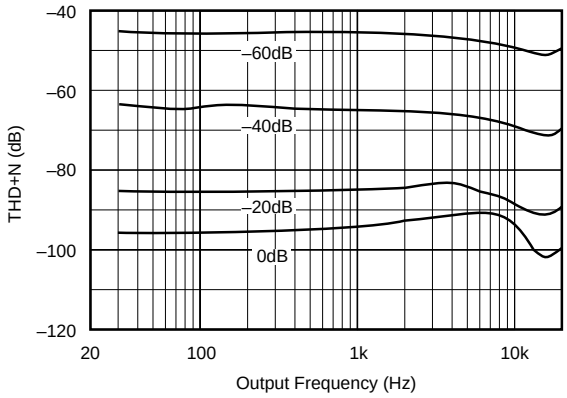
CONNECTION DIAGRAM



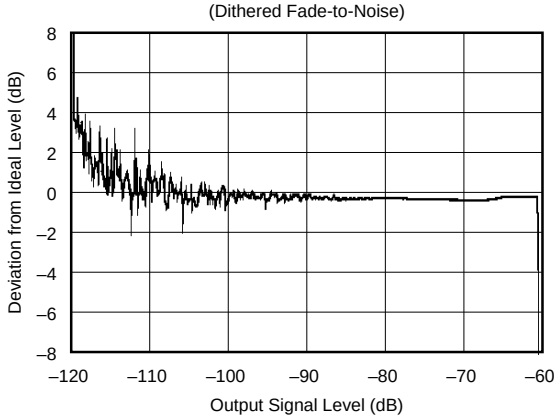
TYPICAL PERFORMANCE CURVES

All specifications at 25°C, $\pm V_A$ and $\pm V_D$ = ±5.0V unless otherwise noted.

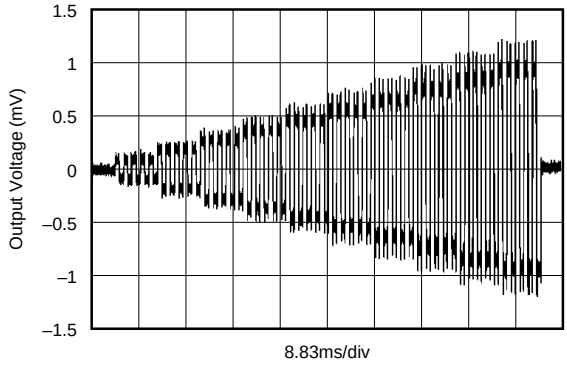
THD+N vs FREQUENCY



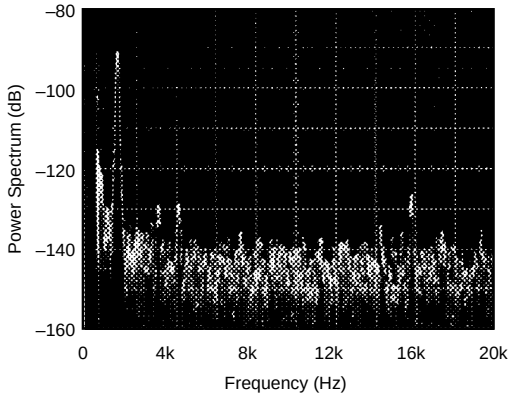
16-BIT LEVEL LINEARITY
(Dithered Fade-to-Noise)



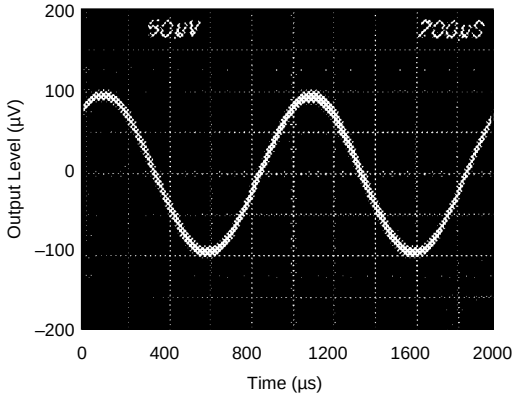
16-BIT MONOTONICITY



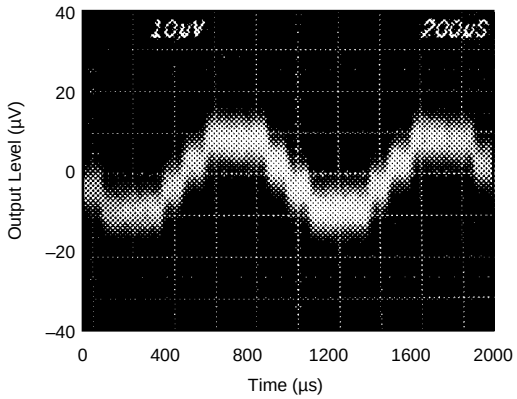
–90dB SIGNAL SPECTRUM
(100Hz Bandwidth)



–90dB SIGNAL
(10Hz to 20kHz Bandwidth)



–110dB SIGNAL
(10Hz to 20kHz Bandwidth)



THEORY OF OPERATION

ADVANCED SIGN MAGNITUDE

Digital audio systems have traditionally used laser-trimmed, current-source DACs in order to achieve sufficient accuracy. However, even the best of these suffer from potential low-level nonlinearity due to errors at the major carry bipolar zero transition. More recently, DACs employing a different architecture which utilizes noise shaping techniques and very high over-sampling frequencies, have been introduced ("Bitstream", "MASH", or 1-bit DAC). These DACs overcome the low level linearity problem, but only at the expense of signal-to-noise performance, and often to the detriment of channel separation and intermodulation distortion if the succeeding circuitry is not carefully designed.

The PCM1702 is a new solution to the problem. It combines all the advantages of a conventional DAC (excellent full scale performance, high signal-to-noise ratio and ease of use) with superior low-level performance. Two DACs are combined in a complementary arrangement to produce an extremely linear output. The two DACs share a common reference, and a common R-2R ladder for bit current sources by dual balanced current segments to ensure perfect tracking under all conditions. By interleaving the individual bits of each DAC and employing precise laser trimming of resistors, the highly accurate match required between DACs is achieved.

This new, complementary linear or advanced sign magnitude approach, which steps away from zero with small steps in both directions, avoids any glitching or "large" linearity errors and provides an absolute current output. The low level performance of the PCM1702 is such that real 20-bit resolution can be realized, especially around the critical bipolar zero point.

Table 1 shows the conversion made by the internal logic of the PCM1702 from binary two's complement (BTC). Also, the resulting internal codes to the upper and lower DACs (see front page block diagram) are listed. Notice that only the LSB portions of either internal DAC are changing around bipolar zero. This accounts for the superlative performance of the PCM1702 in this area of operation.

DISCUSSION OF SPECIFICATIONS

DYNAMIC SPECIFICATIONS

Total Harmonic Distortion + Noise

The key specifications for the PCM1702 is total harmonic distortion plus noise (THD+N).

Digital data words are read into the PCM1702 at eight times the standard compact disk audio sampling frequency of 44.1kHz (352.8kHz) so that a sine wave output of 1002Hz is realized.

For production testing, the output of the DAC goes to an I to V converter, then through a 40kHz low pass filter, and then to a programmable gain amplifier to provide gain at lower signal output test levels before being fed into an analog-type distortion analyzer. Figure 1 shows a block diagram of the production THD+N test setup.

For the audio bandwidth, THD+N of the PCM1702 is essentially flat for all frequencies. The typical performance curve, "THD+N vs Frequency", shows four different output signal levels: 0dB, –20dB, –40dB, and –60dB. The test signals are derived from a special compact test disk (the CBS CD-1). It is interesting to note that the –20dB signal falls only about 10dB below the full scale signal instead of the expected 20dB. This is primarily due to the superior low level signal performance of the advanced sign magnitude architecture of the PCM1702.

In terms of signal measurement, THD+N is the ratio of $Distortion_{RMS} + Noise_{RMS} / Signal_{RMS}$ expressed in dB. For the PCM1702, THD+N is 100% tested at all three specified output levels using the test setup shown in Figure 1. It is significant to note that this test setup does not include any output deglitching circuitry. All specifications are achieved without the use of external deglitchers.

Dynamic Range

Dynamic range in audio converters is specified as the measure of THD+N at an effective output signal level of –60dB referred to 0dB. Resolution is commonly used as a theoretical measure of dynamic range, but it does not take into account the effects of distortion and noise at low signal levels. The advanced sign magnitude architecture of the PCM1702, with its ideal performance around bipolar zero, provides a more usable dynamic range, even using the strict audio definition, than any previously available D/A converter.

ANALOG OUTPUT	INPUT CODE (20-bit Binary Two's Complement)	LOWER DAC CODE (19-bit Straight Binary)	UPPER DAC CODE (19-bit Straight Binary)
+Full Scale	011...111	111...111+1LSB(1)	111...111
+Full Scale –1LSB	011...110	111...111+1LSB(1)	111...110
Bipolar Zero +2LSB	000...010	111...111+1LSB(1)	000...010
Bipolar Zero +1LSB	000...001	111...111+1LSB(1)	000...001
Bipolar Zero	000...000	111...111+1LSB(1)	000...000
Bipolar Zero –1LSB	111...111	111...111	000...000
Bipolar Zero –2LSB	111...110	111...110	000...000
–Full Scale +LSB	100...001	000...001	000...000
–Full Scale	100...000	000...000	000...000

NOTE: (1) The extra weight of 1LSB is added at this point to make the transfer function symmetrical around bipolar zero.

TABLE I. Binary Two's Complement to Sign Magnitude Conversion Chart.

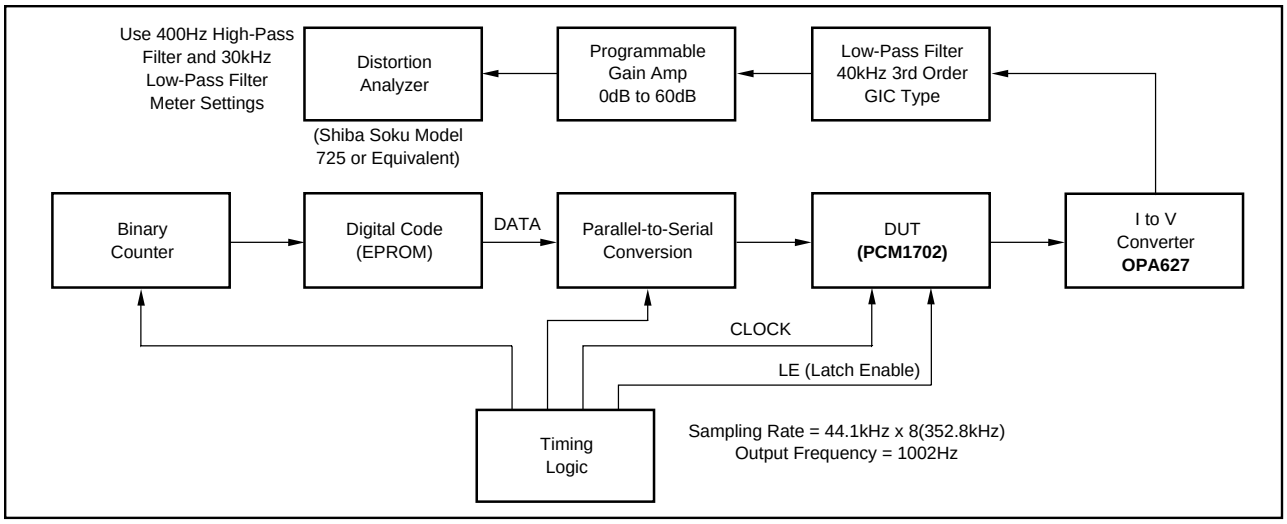


FIGURE 1. Production THD+N Test Setup.

Level Linearity

Deviation from ideal versus actual signal level is sometimes called "level linearity" in digital audio converter testing. See the "–90dB Signal Spectrum" plot in the Typical Performance Curves section for the power spectrum of a PCM1702 at a –90dB output level. (The "–90dB Signal" plot shows the actual –90dB output of the DAC). The deviation from ideal for PCM1702 at this signal level is typically less than ±0.3dB. For the "–110dB Signal" plot in the Typical Performance Curves section, true 20-bit digital code is used to generate a –110dB output signal.

This type of performance is possible only with the low-noise, near-theoretical performance around bipolar zero of the PCM1702 advanced sign magnitude.

A commonly tested digital audio parameter is the amount of deviation from ideal of a 1kHz signal when its amplitude is decreased form –60dB to –120dB. A digitally dithered input signal is applied to reach effective output levels of –120dB using only the available 16-bit code from a special compact disk test input. See the "16-bit Level Linearity" plot in the Typical Performance Curves section for the results of a PCM1702 tested using this 16-bit dithered fade-to-noise signal. Note the very small deviation from ideal as the signal goes from –60dB to –100dB.

DC SPECIFICATION

Idle Channel SNR

Another appropriate specification for a digital audio converter is idle channel signal-to-noise ratio (idle channel SNR). This is the ratio of noise on the DAC output at bipolar zero in relation to the full scale range of the DAC. To make this measurement, the digital input is continuously fed the code for bipolar zero, while the output of the DAC is band-limited from 20Hz to 20kHz and an A-weighted filter is applied. The idle channel SNR for the PCM1702 is typically greater than 120dB, making it ideal for low-noise applications.

Monotonicity

Because of the unique advanced sign magnitude architecture of the PCM1702, increasing values of digital input will always result in increasing values of DAC output as the signal moves away from bipolar zero in one-LSB steps (in either direction). The "16-bit Monotonicity" plot in the Typical Performance Curves section was generated using 16-bit digital code from a test compact disk. The test starts with 10 periods of bipolar zero. Next are 10 periods of alternating 1LSBs above and below zero, and then 10 periods of alternating 2LSBs above and below zero, and so on until 10LSBs above and below zero are reached. The signal pattern then begins again at bipolar zero.

With PCM1702, the low-noise steps are clearly defined and increase in near-perfect proportion. This performance is achieved without any external adjustments. By contrast, sigma-delta ("Bit-stream", "MASH", or 1-bit DAC) architectures are too noisy to even see the first 3 or 4 bits change (at 16 bits), other than by a change in the noise level.

Absolute Linearity

Even though absolute integral and differential linearity specs are not given for the PCM1702, the extremely low THD+N performance is typically indicative of 17-bit integral linearity in the DAC. The relationship between THD+N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

Offset, Gain, and Temperature Drift

Although the PCM1702 is primarily meant for use in dynamic applications, specifications are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain and offset drift.

DIGITAL INPUT

Timing Considerations

The PCM1702 accepts TTL compatible logic input levels. The data format of the PCM1702 is binary two's complement (BTC) with the most significant bit (MSB) being first

in the serial input bit stream. Table II describes the exact relationship of input data to voltage output coding. Any number of bits can precede the 20 bits to be loaded, since only the last 20 will be transferred to the parallel DAC register after Latch Enable (Pin6 <PCM1702P>, Pin7 <PCM1702U>, LE) has gone low.

All DAC serial input data (Pin1, DATA) bit transfers are triggered on positive clock (Pin2, CLOCK), edges. The serial-to-parallel data transfer to the DAC occurs on the falling edge of Latch Enable. The change in the output of the DAC occurs at a rising edge of the 4th clock of the CLOCK after the falling edge of Latch Enable. Refer to Figure 2 for graphical relationships of these signals.

Maximum Clock Rate

A typical clock rate of 16.9MHz for the PCM1702 is derived by multiplying the standard audio sample rate of 44.1kHz by sixteen times (16X over-sampling) the standard audio word bit length of 24 bits (44.1kHz x 16 x 24 = 16.9MHz). Note that this clock rate accommodates a 24-bit word length, even though only 20 bits are actually being used. The setup and hold timing relationships are shown in Figure 3.

"Stopped Clock" Operation

The PCM1702 is normally operated with a continuous clock input signal. If the clock is to be stopped between input data words, the last 20 bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until Latch Enable goes low. Latch Enable must remain low until after the first clock cycle of the next data word to insure proper DAC operation. In any case, the setup and hold times for Data and LE must be observed as shown in Figure 3.

DIGITAL INPUT	ANALOG OUTPUT	CURRENT OUTPUT
1,048,576LSBs	Full Scale Range	2.40000000mA
1LSB	NA	2.28882054nA
$7FFFF_{HEX}$	+Full Scale	–1.19999771mA
00000_{HEX}	Bipolar Zero –1LSB	0.00000000mA
80000_{HEX}	–Full Scale	+1.20000000mA

TABLE II. Digital Input/Output Relationships.

INSTALLATION

POWER SUPPLIES

Refer to CONNECTION DIAGRAM for proper connection of the PCM1702. The PCM1702 only requires a ±5V supply. Both positive supplies should be tied together at a single point. Similarly, both negative supplies should be connected together. No real advantage is gained by using separate analog and digital supplies. It is more important that both these supplies be as "clean" as possible to reduce coupling of supply noise to the output. Power supply decoupling capacitors should be used at each supply pin to maximize power supply rejection, as shown in CONNECTION DIAGRAM regardless of how good the supplies are. Both commons should be connected to an analog ground plane as close to the PCM1702 as possible.

FILTER CAPACITOR REQUIREMENTS

As shown in CONNECTION DIAGRAM, various size decoupling capacitors can be used, with no special tolerances being required. The size of the offset decoupling capacitor is not critical either, with larger values (up to 100µF) giving slightly better SNR readings. All capacitors should be as close to the appropriate pins of the PCM1702 as possible to reduce noise pickup from surrounding circuitry.

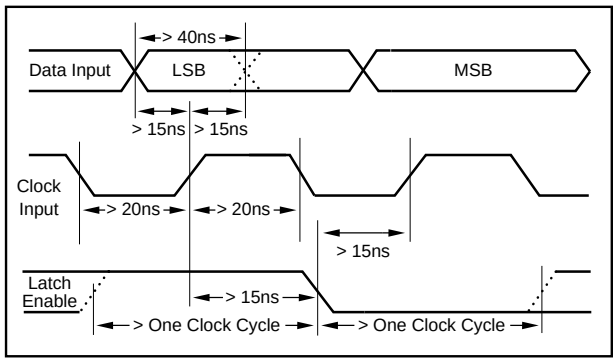
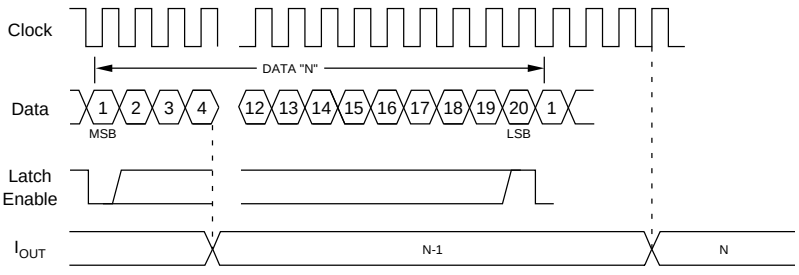


FIGURE 3. Setup and Hold Timing Diagram.



NOTES : (1) If clock is stopped between input of 20-bit data words, "Latch" Enable (LE) must remain low until after the first clock cycle of the next 20-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch Enable (LE) must remain low at least one clock cycle after going negative. (4) Latch Enable (LE) must be high for at least one clock cycle before going negative. (5) I_{OUT} changes on positive going edge of the 4th clock after negative going edge of Latch Enable (LE).

FIGURE 2. Timing Diagram.

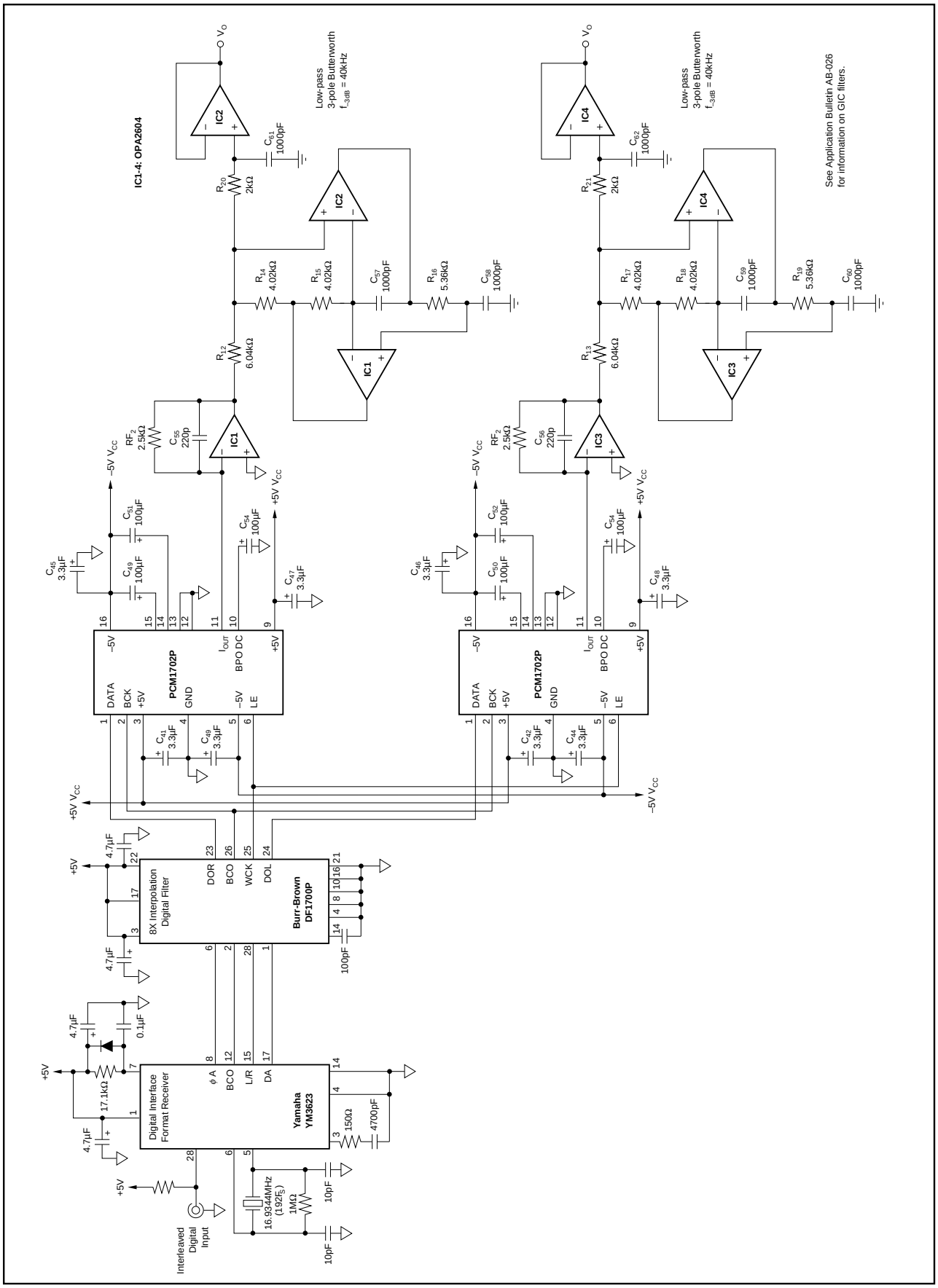


FIGURE 4. Typical Application for Stereo Audio 8X Oversampling system.