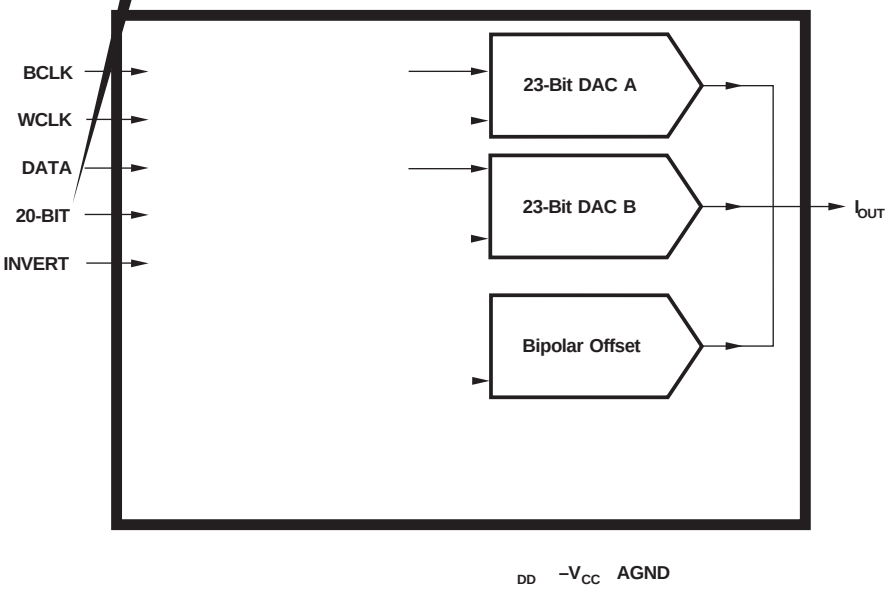
BURR - BROWN®

PCM1704

24-Bit, 96kHz BiCMOS Sign-Magnitude DIGITAL-TO-ANALOG CONVERTER

FEATURES

- SAMPLING FREQUENCY (f_S): 16kHz to 96kHz
- 8X OVERSAMPLING AT 96kHz
- INPUT AUDIO DATA WORD: 20- or 24-Bit
- HIGH PERFORMANCE:
  Dynamic Range: K Grade = 122dB typ
  SNR: 120dB typ
  THD+N: K Grade = 0.0008% typ
- FAST CURRENT OUTPUT: ±1.2mA/200ns
- GLITCH-FREE OUTPUT
- PIN-PROGRAMMABLE DATA INVERSION
- PERFECT CHANNEL-TO-CHANNEL MATCHING



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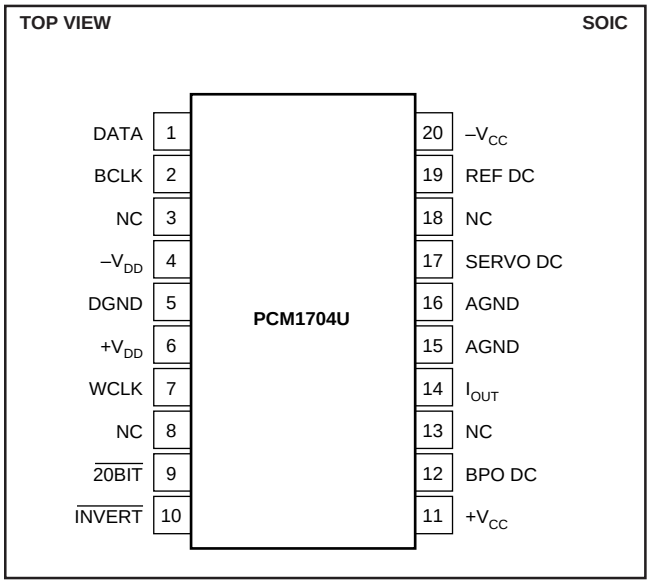
SPECIFICATIONS

All specifications at T_A = +25°C, $\pm V_{CC} = \pm V_{DD} = \pm 5V$, f_S = 768kHz (96kHz • 8), and 24-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1704U MIN	PCM1704U TYP	PCM1704U MAX	UNITS
RESOLUTION			24		Bits
DATA FORMAT					
Audio Data Interface Format			20-, 24-Bit, MSB-First		
Audio Data Code			Binary Two's Complement		
Sampling Frequency (f_S)		16		96	kHz
Input Clock Frequency				25	MHz
DIGITAL INPUT/OUTPUT					
Input Logic Level:					
V_{IH}(1)		+2.0		+5.0	V
V_{IL}(1)		0		+0.8	V
V_{IH}(2)		–3.0		0	V
V_{IL}(2)		–5.0		–4.2	V
Input Logic Current:					
I_{IH}(1)	$V_{IH} = +V_{DD}$			±10	µA
I_{IL}(1)	V_{IL} = 0V			±10	µA
I_{IH}(2)	V_{IH} = 0V			±10	µA
I_{IL}(2)	$V_{IL} = -V_{DD}$			–100	µA
DYNAMIC PERFORMANCE(3)					
THD+N V_O = 0dB	PCM1704U		0.0025	0.0030	%
	PCM1704U-J		0.0015	0.0025	%
	PCM1704U-K		0.0008	0.0015	%
V_O =–20dB	PCM1704U		0.008	0.020	%
	PCM1704U-J		0.007	0.015	%
	PCM1704U-K		0.006	0.01	%
Dynamic Range	EIAJ, A-weighted				
	PCM1704U, U-J	102	110		dB
	PCM1704U-K	106	112		dB
Signal-to-Noise Ratio	EIAJ, A-weighted	112	120		dB
Low Level Linearity	f = 1002Hz at –90dB		±0.5		dB
DC ACCURACY					
Gain Error			±1.0	±3.0	% of FSR
Bipolar Zero Error			±0.5	±1.0	% of FSR
Gain Drift	0°C to 70°C		±25		ppm of FSR/°C
Bipolar Zero Error Drift	0°C to 70°C		±5		ppm of FSR/°C
ANALOG OUTPUT					
Output Range			±1.2		mA
Output Impedance			1.0		kΩ
Settling Time	±0.0003% of FSR, ±1.2mA Step		200		ns
POWER SUPPLY REQUIREMENTS					
Voltage Range: $+V_{CC} = +V_{DD}$		+4.75	+5.0	+5.25	VDC
$-V_{CC} = -V_{DD}$		–4.75	–5.0	–5.25	VDC
Combined Supply Current: $+I_{CC}$	$+V_{CC} = +V_{DD} = +5.0V$		5	8	mA
$-I_{CC}$	$-V_{CC} = -V_{DD} = -5.0V$		30	45	mA
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+125	°C

NOTES: (1) BCLK, WCLK, DATA. (2) $\overline{20BIT}$, $\overline{INVERT}$. (3) Dynamic performance data is tested with 5534 I/V amp with 7.5kΩ feedback resistor. THD+N data is tested by Shibasoku 725C with 30kHz external LPF, 400Hz HPF, average mode. Input signal frequency = 1.1kHz.

PIN CONFIGURATION



PACKAGE INFORMATION

PRODUCT	PACKAGE	TEMPERATURE RANGE	PACKAGE DRAWING NUMBER(1)
PCM1704U	20-Lead SOIC	–25°C to +85°C	248

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_{DD}$, $+V_{CC}$	+6.5V
Supply Voltage Differences	±0.1V
GND Voltage Differences	±0.1V
Digital Input Voltage	
(BCLK, WCLK, DATA)	DGND –0.3V to ($+V_{DD}$ + 0.3V)
($\overline{20BIT}$, $\overline{INVERT}$)	$-V_{DD}$ – 0.3V to (DGND + 0.3V)
Input Current (any pins except supply pins)	±10mA
Power Dissipation	300mW
Operating Temperature Range	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Package Temperature (reflow, 10s)	+235°C

PIN ASSIGNMENTS

PIN	NAME	I/O	FUNCTION
1	DATA	IN	Serial Audio Data Input.
2	BCLK	IN	Bit Clock Input for Serial Audio Data.
3	NC	—	No Connection.
4	$-V_{DD}$	—	Digital Power, –5V.
5	DGND	—	Digital Ground.
6	$+V_{DD}$	—	Digital Power, +5V.
7	WCLK	IN	Data Latch Enable Input.
8	NC	—	No Connection.
9	$\overline{20BIT}$	IN	Input Data Word Selection(1).
10	$\overline{INVERT}$	IN	Input Data Polarity Selection(1).
11	$+V_{CC}$	—	Analog Power, +5V.
12	BPO DC	—	Bipolar Offset Decoupling Capacitor.
13	NC	—	No Connection.
14	I_{OUT}	OUT	Current Output for Audio Signal.
15	AGND	—	Analog Ground.
16	AGND	—	Analog Ground.
17	SERVO DC	—	Servo Amplifier Decoupling Capacitor.
18	NC	—	No Connection.
19	REF DC	—	Band Gap Reference Decoupling Capacitor.
20	$-V_{CC}$	—	Analog Power, –5V.

NOTE: (1) Internal pull-up resistors. Input level must be a voltage from $-V_{DD}$ to DGND.

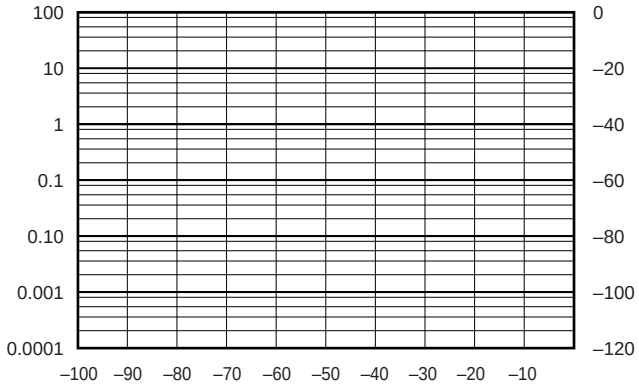
ELECTROSTATIC DISCHARGE SENSITIVITY

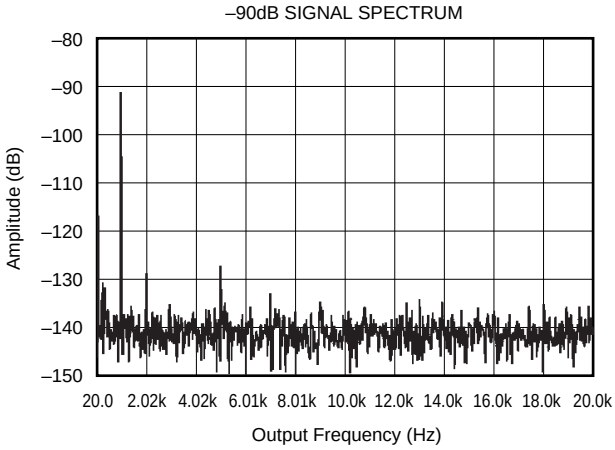
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

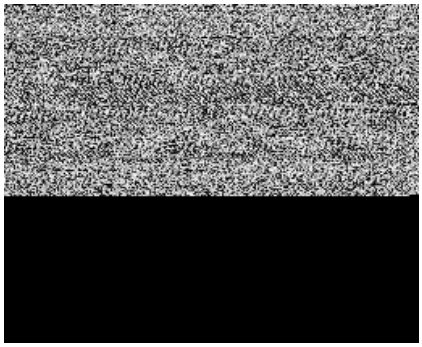
SPECIFICATIONS

All specifications at +25°C, $\pm V_{CC}$ and $\pm V_{DD}$ = ±5.0V, unless otherwise noted.



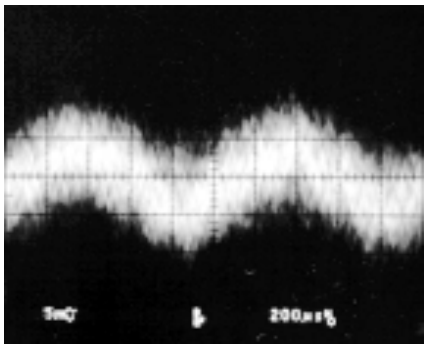


DAC OUTPUT
–110dB, 24-Bit, 96kHz

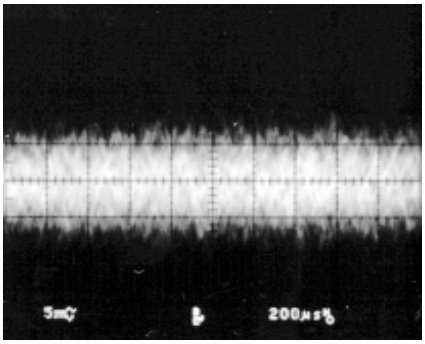


DAC OUTPUT
–110dB, 20-Bit, 96kHz

DAC OUTPUT
–120dB, 24-Bit, 96kHz

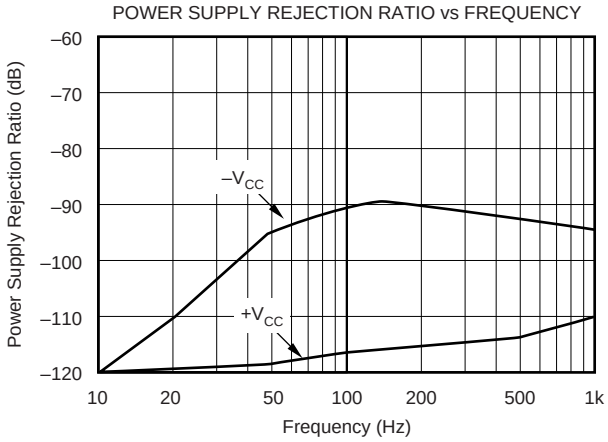


DAC OUTPUT
–120dB, 20-Bit, 96kHz



SPECIFICATIONS (CONT)

All specifications at +25°C, $\pm V_{CC}$ and $\pm V_{DD}$ = ±5.0V, unless otherwise noted.



THEORY OF OPERATION

SIGN-MAGNITUDE ARCHITECTURE

Digital audio systems have traditionally used laser-trimmed, current-source DACs in order to achieve sufficient accuracy. However, even the best of these suffer from potential low-level nonlinearity due to errors in the major carry bipolar zero transition. Current systems have turned to oversampling data converters, such as the popular delta-sigma architectures, to correct the linearity problems. This is done, however, at the expense of signal-to-noise performance, and the noise shaping techniques utilized by these converters creates a considerable amount of out-of-band noise. If the outputs are not properly filtered, dynamic performance of the overall system will be adversely effected.

The PCM1704 employs an innovative architecture which combines the advantages of traditional DACs (e.g., excellent full-scale performance, high signal-to-noise ratio, and ease of use) with superior low-level performance. This architecture is referred to as sign-magnitude. Two DACs are combined in a complementary arrangement to produce an extremely linear output. The two DACs share a common reference, and a common R-2R ladder for bit current sources. The R-2R ladder utilizes dual balanced current segments to ensure ideal tracking under all conditions. By interleaving the individual bits of each DAC and employing precision laser-trimming of resistors, a highly accurate match between the two DACs is achieved.

The sign-magnitude architecture, which steps away from zero with small steps in both directions, avoids any glitching or large linearity errors, and provides an absolute current output. The low-level performance of the PCM1704 is such that true 24-bit resolution can be realized around the critical bipolar zero point.

DISCUSSION OF KEY SPECIFICATIONS

TOTAL HARMONIC DISTORTION + NOISE (THD+N)

This is the key specification for the PCM1704. Digital data words are read into the PCM1704 at eight times the standard DVD audio sampling frequency of 96kHz (e.g., 8 x 96kHz = 768kHz) to create a sinewave output of 1100Hz. The output of the DAC is then passed through analog signal conditioning circuitry before being input to a distortion analyzer.

For production testing, the output of the DAC is connected to a current-to-voltage (I/V) converter. The output of the I/V converter is then connected to a 40kHz, 3rd-order GIC low-pass filter. The filter output is then passed on to a programmable gain amplifier to provide gain for low-level test signals before being fed into an analog distortion analyzer (Shiba Soku Model 725 or equivalent).

For the audio bandwidth, the THD+N for the PCM1704 is essentially flat for all frequencies.

DYNAMIC RANGE

Dynamic range in data converters is specified as the measure of THD+N at an effective output signal level of –60dBFS (conforms to EIAJ method with A-weighting applied). Resolution is commonly used as a theoretical measure of dynamic range, but it does not take into account the effects of distortion and noise at low signal levels. The sign-magnitude architecture of the PCM1704, with its ideal performance around bipolar zero, provides a more usable dynamic range (even with the strict audio definition) than any other previously available D/A converter.

IDLE CHANNEL SIGNAL-TO-NOISE RATIO (SNR)

Another important specification for a digital audio converter is idle channel signal-to-noise ratio (Idle Channel SNR). This is the ratio of the noise on the DAC output at bipolar zero compared to the full-scale range of the D/A converter. To make this measurement, the digital input is continually fed the code for bipolar zero, while the output of the DAC is band limited from 20Hz to 20kHz and A-weighting is applied. The ideal channel SNR for the PCM1704 is typically greater than 120dB, making it ideal for low noise applications.

OFFSET GAIN AND TEMPERATURE DRIFT

Although the PCM1704's primary application is in high performance digital audio systems where dynamic specifications are most important, specifications are also given for more traditional DC parameters. These include gain error, bipolar zero offset, temperature gain and offset drift. These specifications are important in test and measurement systems, which is the other main systems application for the PCM1704.

AUDIO DATA INTERFACE

BASIC OPERATION

The audio interface of the PCM1704 accepts TTL-compatible input levels. The data format at the DATA input of the PCM1704 is Binary Two's Complement, with the most significant bit (MSB) being first in the serial input bit steam. Table I shows the relationship between the audio input data and DAC output for the PCM1704. Any number of bits can precede the 24 bits to be loaded since only the last 24 bits will be transferred to the parallel DAC register after WCLK (pin 7) has gone LOW (logic 0).

BINARY TWO'S COMPLEMENT INPUT DATA (Hex)	DAC OUTPUT
7FFFFF	+ Full Scale
000000	Bipolar Zero
FFFFFF	Bipoar Zero – 1 LSB
800000	– Full Scale

TABLE I. Digital Input/DAC Output Relationships.

Audio data is supplied to the DATA (pin 1) input. The bit clock is used to shift data into the PCM1704 and is supplied to BCLK (pin 2). All DAC serial input data bits are latched into the serial input register on the rising edge of BCLK. The serial-to-parallel data transfer to the DAC occurs on the falling edge of WCLK. The change in the output of the DAC occurs at the rising edge of the 2nd BCLK after the falling edge of WCLK. Figure 1 shows the audio data input format. Figure 2 shows the input timing relationships.

Maximum Bit Clock (BCLK) Rate

The maximum BCLK rate is specified as 25MHz. This is derived from the 8X oversampling of the PCM1704. Given a 96kHz sampling rate, an 8X oversampling input and a 32-bit frame length, we get:

96kHz • 8 • 32 = 24.576MHz

"Stopped Clock" Operation

The PCM1704 is normally operated with a continuous BCLK input. If BCLK is stopped between input data words, the last 24 bits shifted in are not actually transferred from the serial register to the parallel DAC register until WCLK goes LOW. WCLK must remain LOW until after the first BCLK cycle of the next data word to insure proper DAC operation. The specified setup and hold times for DATA and WCLK must be observed.

DATA FORMAT CONTROL

Data format is controlled by two pins on the PCM1704—the $\overline{20BIT}$ and $\overline{INVERT}$ inputs. Their functions are described in the following paragraphs and tables.

Input Word Length

20BIT (pin 9) is used to select the input data length. Table II shows the available selections. Pin 9 is internally pulled up to DGND and therefore, defaults to 24-bit data.

$\overline{20BIT}$ (Pin 9)	DATA WORD LENGTH
$\overline{20BIT}$ = H (DGND)	24-Bit Data Word
$\overline{20BIT}$ = L ($-V_{DD}$)	20-Bit Data Word

TABLE II. Input Word Length Selection.

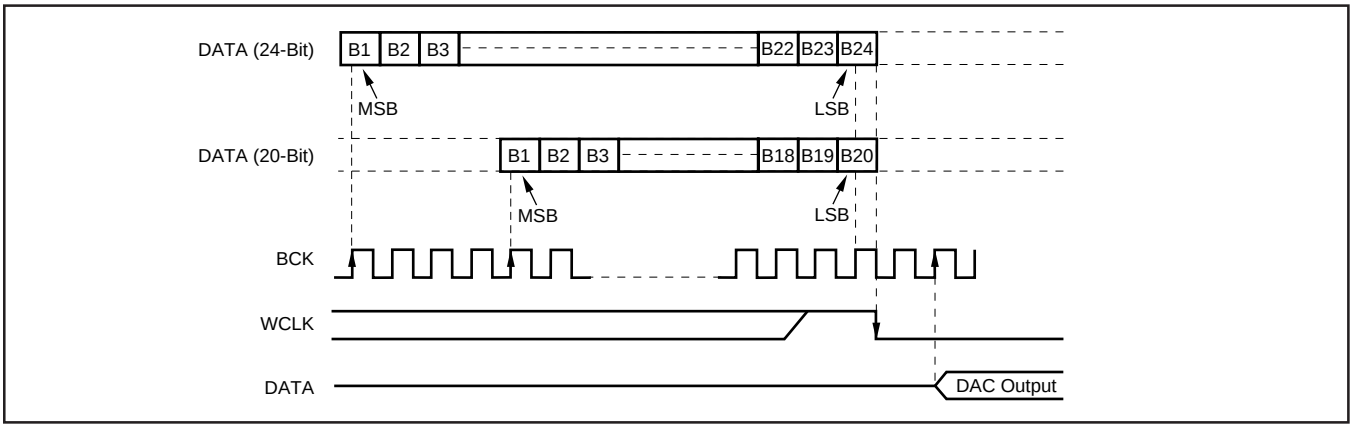
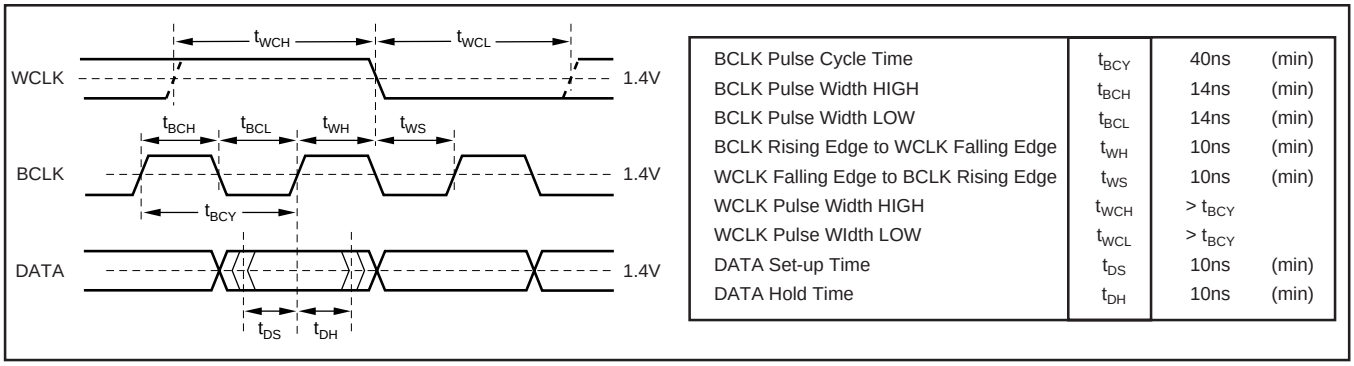


FIGURE 1. Audio Input Data Format.



BCLK Pulse Cycle Time	t_{BCY}	40ns	(min)
BCLK Pulse Width HIGH	t_{BCH}	14ns	(min)
BCLK Pulse Width LOW	t_{BCL}	14ns	(min)
BCLK Rising Edge to WCLK Falling Edge	t_{WH}	10ns	(min)
WCLK Falling Edge to BCLK Rising Edge	t_{WS}	10ns	(min)
WCLK Pulse Width HIGH	t_{WCH}	> t_{BCY}	
WCLK Pulse WIdth LOW	t_{WCL}	> t_{BCY}	
DATA Set-up Time	t_{DS}	10ns	(min)
DATA Hold Time	t_{DH}	10ns	(min)

FIGURE 2. Audio Input Data Timing.

Input Data Inversion

$\overline{\text{INVERT}}$ (pin 10) is used to select the phase of the input data presented to the DAC. Table III shows the two options. Pin 10 is internally pulled up to DGND, and therefore defaults to normal, or non-inverting data.

$\overline{\text{INVERT}}$ (Pin 10)	PHASE
$\overline{\text{INVERT}}$ = H (DGND)	Normal (non-inverted)
$\overline{\text{INVERT}}$ = L ($-V_{DD}$)	Inverted

TABLE III. Input Data Phase Selection.

APPLICATIONS INFORMATION

POWER SUPPLIES

For this discussion, please refer to the internal connection diagram for the PCM1704 in Figure 3. The PCM1704 only requires a ±5V supply for operation. Both positive supplies ($+V_{DD}$ and $+V_{CC}$) should be tied together at a single point and connected to a single +5V analog power supply. Similarly, both negative supplies ($-V_{DD}$ and $-V_{CC}$) should be tied at a single point and connected to a single –5V analog power supply. No advantage is gained by using separate analog and digital power supplies. It is more important that the analog supplies used to drive these pins are as noise and ripple free as possible to reduce coupling of supply noise to the output.

Power supply decoupling capacitors should be used at each supply pin to maximize power supply rejection, as shown in Figure 3. All ground pins (AGND and DGND) should be connected to an analog ground plane as close to the PCM1704 as possible. The PCM1704 should reside entirely over the analog ground plane of the printed circuit board.

Bypass and Decoupling Capacitor Requirements

Various-sized decoupling capacitors can be used, with no special tolerances being required. Figure 5 shows typical values used by Burr-Brown on our evaluation fixture, which designers can use as recommended values. All capacitors should be located as close to the appropriate pins of the PCM1704 as possible to reduce noise pickup from surrounding circuitry. Aluminum electrolytic capacitors are recommended for larger values, while metal-film or monolithic ceramic capacitors are used for smaller values.

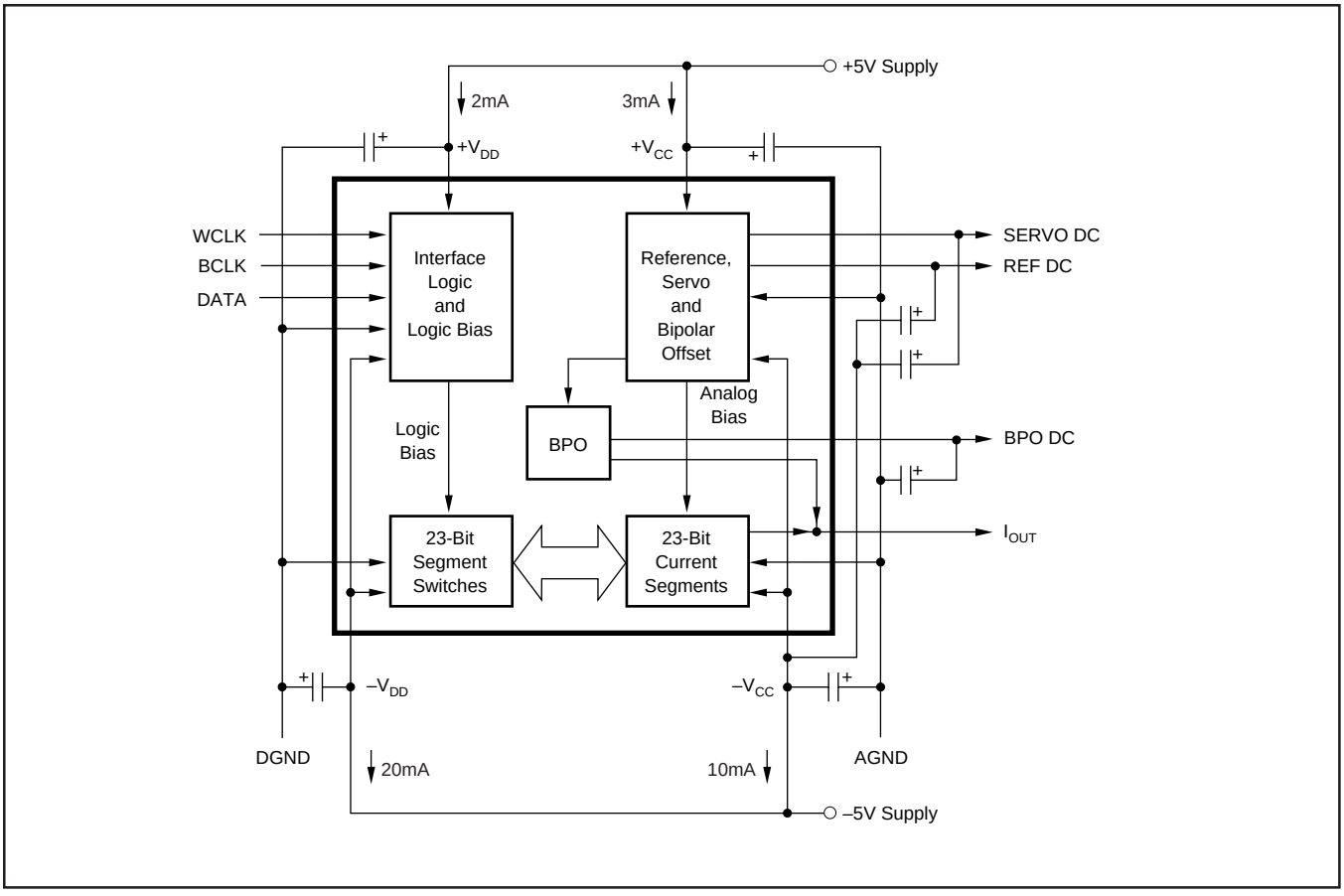


FIGURE 3. PCM1704 Internal Connection Diagram.

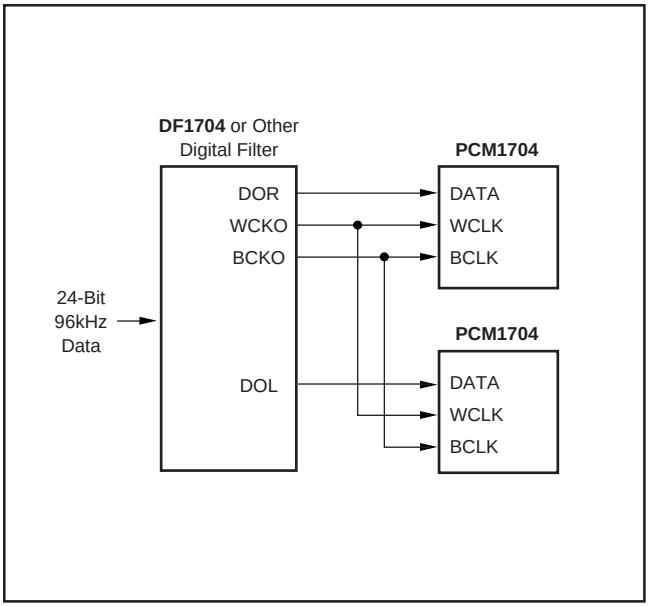


FIGURE 4. Audio Interface Connections for Stereo Audio Application.

TYPICAL APPLICATION EXAMPLES

The audio interface connections for a stereo audio application is shown in Figure 4. The audio data is input to the digital filter, which then oversampleS the data by a factor of 8. The audio data is then filtered digitally and output to the PCM1704 DACs.

Figure 5 shows single channel circuit connections for a typical PCM1704 application. It shows the PCM1704 interface to the digital filter, the I/V converter, and the DAC post filter. Selection of an appropriate op amp for the I/V converter is critical for obtaining optimum dynamic performance from the PCM1704. The OPA627 is recommended for this application. Op amps with similar characteristics and faster settling times may also be used.

The suggested DAC post filter is a second-order lowpass active filter, using the multiple feedback (MFB) circuit technique. The OPA2134 is an excellent choice for the op amp in this circuit, since it is designed for high performance audio applications. The post filter is used to reconstruct and band limit the DAC output signal.

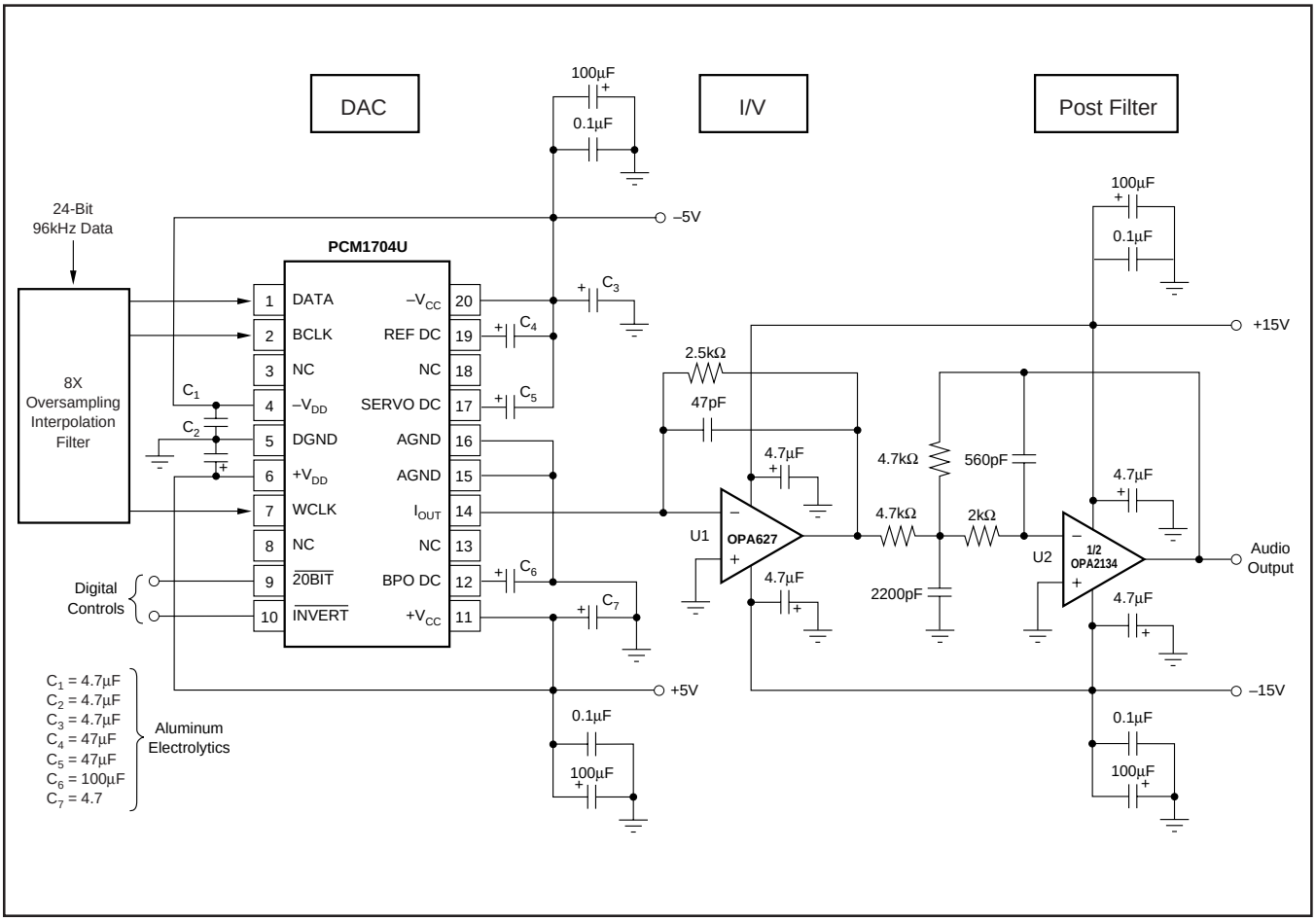


FIGURE 5. Typical Application Circuit (one channel shown).

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
PCM1704U	ACTIVE	SOP	NS	20	38
PCM1704U-J	ACTIVE	SOP	NS	20	38
PCM1704U-J/2K	ACTIVE	SOP	NS	20	2000
PCM1704U-K	ACTIVE	SOP	NS	20	38
PCM1704U-K/2K	ACTIVE	SOP	NS	20	2000
PCM1704U/2K	ACTIVE	SOP	NS	20	2000
PCM1704UNB	ACTIVE	SOP	NS	20	38

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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