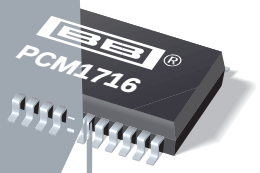
PCM1716



24-Bit, 96kHz Sampling Delta-Sigma Stereo Audio DIGITAL-TO-ANALOG CONVERTER

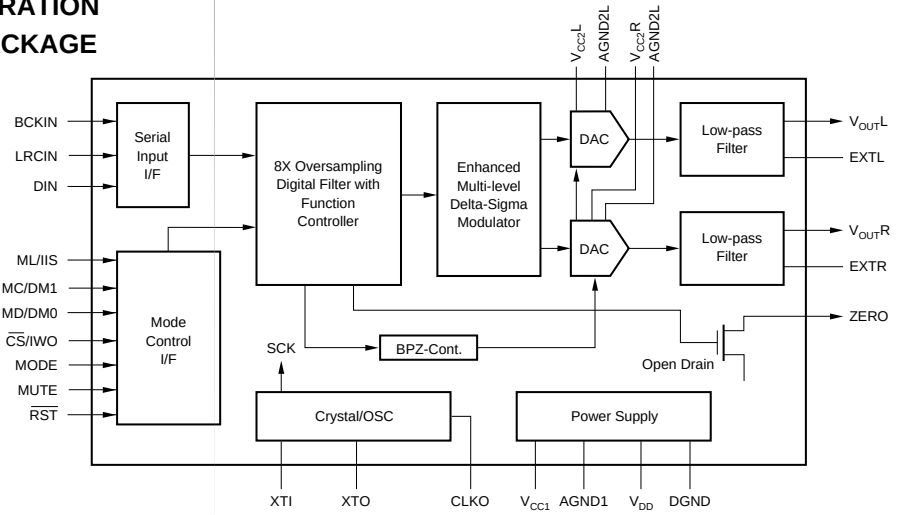
- **DELTA-SIGMA DAC**
- **Sampling: 16kHz - 96kHz**
- **SNR: 106dB**
- **Dynamic Range: 106dB**
- **Output Range: 0.62 x V_{CC} (Vp-p)**
- **OVERSAMPLING DIGITAL FILTER:**
  - **Stop Band Attenuation: –82dB**
  - **Pass Band Ripple: ±0.002dB**
  - **Sharp Roll Off**
- **MULTI FUNCTIONS:**
  - **Digital De-emphasis**
  - **L/R Independent Digital Attenuation**
  - **Soft Mute**
  - **Zero Detect Mute**
  - **Zero Flag**
  - **Chip Select**
  - **Reversible Output Phase**
- **+5V SINGLE SUPPLY OPERATION**
- **SMALL 28-LEAD SSOP PACKAGE**

DESCRIPTION

The PCM1716 is designed for Mid to High grade Digital Audio applications which achieve 96kHz sampling rates with 24-bit audio data. PCM1716 uses a newly developed, enhanced multi-level delta-sigma modulator architecture that improves audio dynamic performance and reduces jitter sensitivity in actual applications.

The internal digital filter operates at 8x over sampling at a 96kHz sampling rate, with two kinds of roll-off performances that can be selected: sharp roll-off, or slow roll-off, as required for specific applications.

PCM1716 is suitable for Mid to High grade audio applications such as CD, DVD-Audio, and Music Instruments, since the device has superior audio dynamic performance, 24-bit resolution and 96kHz sampling.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1415C
Printed in U.S.A. August, 1998
SBAS080

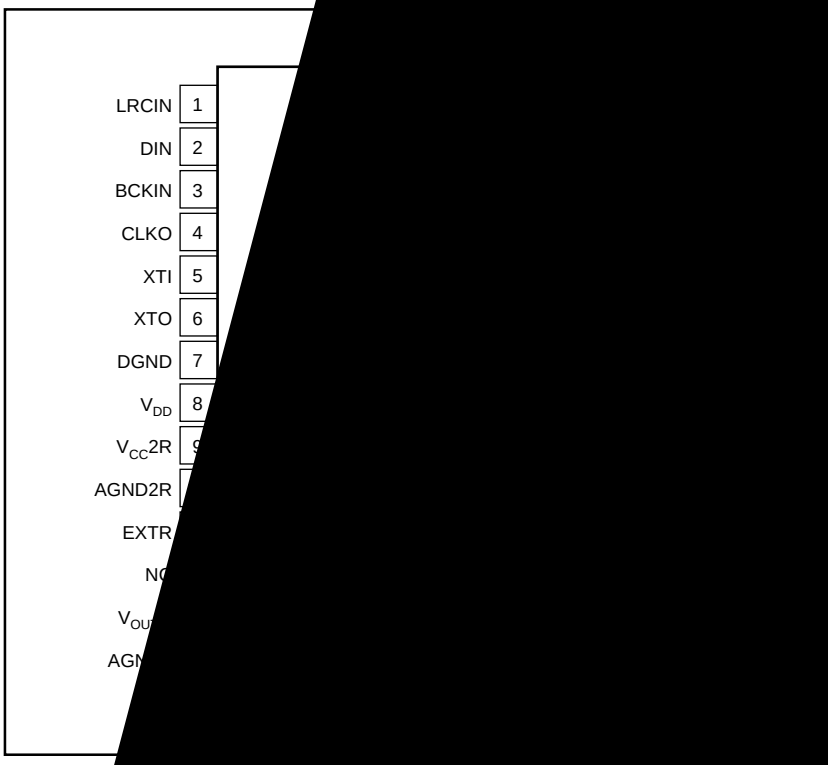
SPECIFICATIONS

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, and 24-bit input data, SYSCLK = 384f_S, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1716 MIN	PCM1716 TYP	PCM1716 MAX	UNITS
RESOLUTION			24		Bits
DATA FORMAT					
Audio Data Interface Format			Standard/I²S		
Data Bit Length			16/20/24 Selectable		
Audio Data Format			MSB First, 2's Comp		
Sampling Frequency (f_S)		16		96	kHz
System Clock Frequency(1)			256/384/512/768f_S		
DIGITAL INPUT/OUTPUT LOGIC LEVEL					
Input Logic Level V_{IH}		2.0			V
V_{IL}				0.8	V
Output Logic Level (CLKO) V_{OH}	I_{OH} = 2mA	4.5			V
V_{OL}	I_{OL} = 4mA			0.5	V
CLKO PERFORMANCE(2)					
Output Rise Time	20 ~ 80% V_{DD}, 10pF		5.5		ns
Output Fall Time	80 ~ 20% V_{DD}, 10pF		4		ns
Output Duty Cycle	10pF Load		37		%
DYNAMIC PERFORMANCE(3) (24-Bit Data)					
THD+N V_O = 0dB	f_S = 44.1kHz		–97	–90	dB
	f_S = 96kHz		–94		dB
V_O = –60dB	f_S = 44.1kHz		–42		dB
Dynamic Range	f_S =44.1kHz EIAJ A-weighted	98	106		dB
	f_S = 96kHz A-weighted		103		dB
Signal-to-Noise Ratio(4)	f_S =44.1kHz EIAJ A-weighted	98	106		dB
	f_S = 96kHz A-weighted		103		dB
Channel Separation	f_S = 44.1kHz	96	102		dB
	f_S = 96kHz		101		dB
DYNAMIC PERFORMANCE(3) (16-Bit Data)					
THD+N V_O = 0dB	f_S = 44.1kHz		–94		dB
	f_S = 96kHz		–92		dB
Dynamic Range	f_S = 44.1kHz EIAJ A-weighted		98		dB
	f_S = 96kHz A-weighted		97		dB
DC ACCURACY					
Gain Error			±1.0	±3.0	% of FSR
Gain Mismatch: Channel-to-Channel			±1.0	±3.0	% of FSR
Bipolar Zero Error	V_O = 0.5V_{CC} at Bipolar Zero		±30	±60	mV
ANALOG OUTPUT					
Output Voltage	Full Scale (0dB)		0.62 V_{CC}		Vp-p
Center Voltage			0.5 V_{CC}		V
Load Impedance	AC Load	5			kΩ
DIGITAL FILTER PERFORMANCE					
Filter Characteristics 1					
(Sharp Roll-Off)					
Passband	±0.002dB			0.454f_S	
	–3dB			0.490f_S	
Stopband		0.546f_S			
Passband Ripple				±0.002	dB
Stopband Attenuation	Stop Band = 0.546f_S	–75			dB
	Stop Band = 0.567f_S	–82			dB
Filter Characteristics 2					
(Slow Roll-Off)					
Passband	±0.002dB			0.274f_S	
	–3dB			0.454f_S	
Stopband		0.732f_S			
Passband Ripple				±0.002	dB
Stopband Attenuation	Stopband = 0.732f_S	–82			dB
Delay Time			30/f_S		sec
De-emphasis Error				±0.1	dB
INTERNAL ANALOG FILTER					
–3dB Bandwidth			100		kHz
Passband Response	f = 20kHz		–0.16		dB
POWER SUPPLY REQUIREMENTS					
Voltage Range	V_{DD}, V_{CC}	4.5	5	5.5	VDC
Supply Current: I_{CC} +I_{DD}	f_S = 44.1kHz		32	45	mA
	f_S = 96kHz		45		mA
Power Dissipation	f_S = 44.1kHz		160	225	mW
	f_S = 96kHz		225		mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTES: (1) Refer section of system clock. (2) External buffer is recommended. (3) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average Mode. (4) SNR is tested at internally infinity zero detection off.

PIN CONFIGURATION



PACKA

PRODU
PCM1

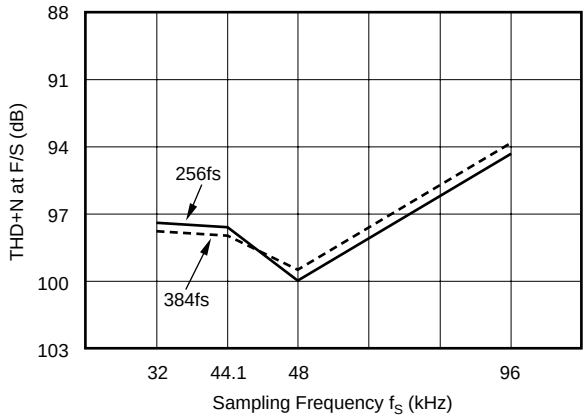
NOTE:
sheet,

AB

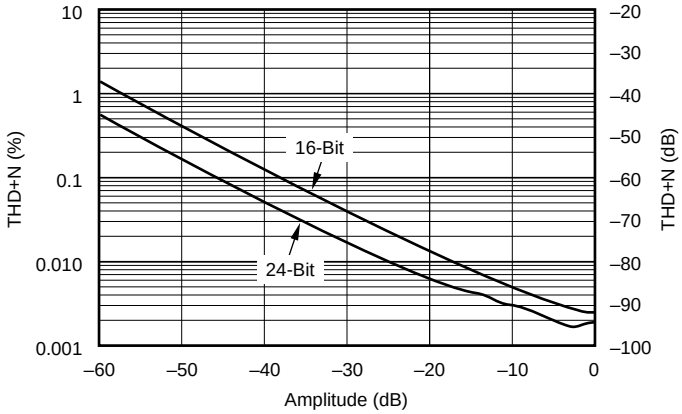
TYPICAL PERFORMANCE CURVES

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, and 24-bit input data, SYSCLK = 384f_S, unless otherwise noted.

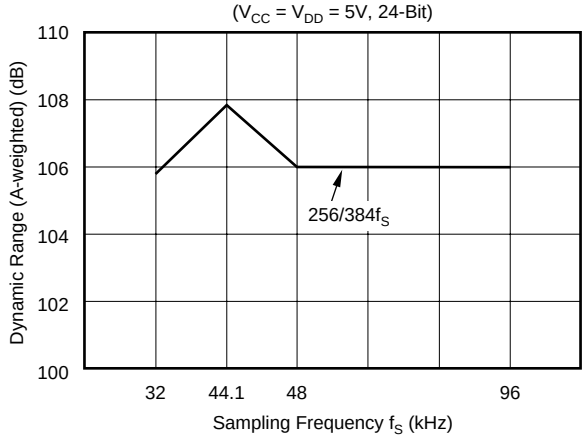
THD+N vs SAMPLING FREQUENCY
(V_{CC} = V_{DD} = 5V, 24-Bit)



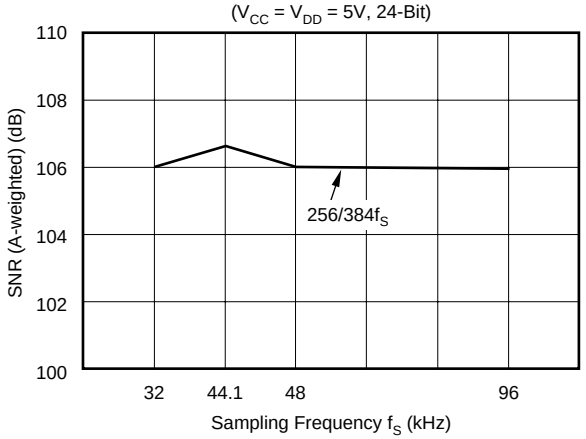
THD+N vs LEVEL
(f_S = 44.1kHz)



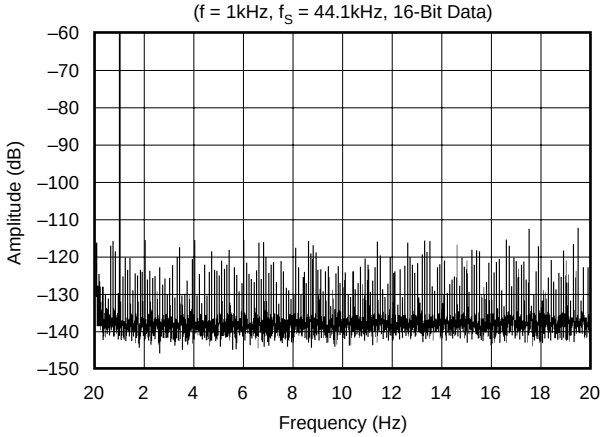
DYNAMIC RANGE vs SAMPLING FREQUENCY
(V_{CC} = V_{DD} = 5V, 24-Bit)



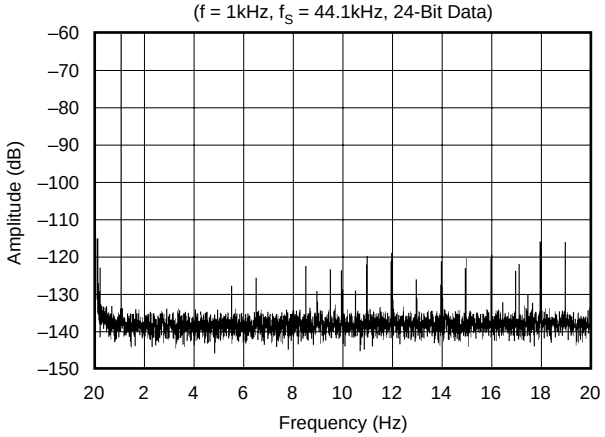
SNR vs SAMPLING FREQUENCY
(V_{CC} = V_{DD} = 5V, 24-Bit)



–60dB OUTPUT SPECTRUM
(f = 1kHz, f_S = 44.1kHz, 16-Bit Data)

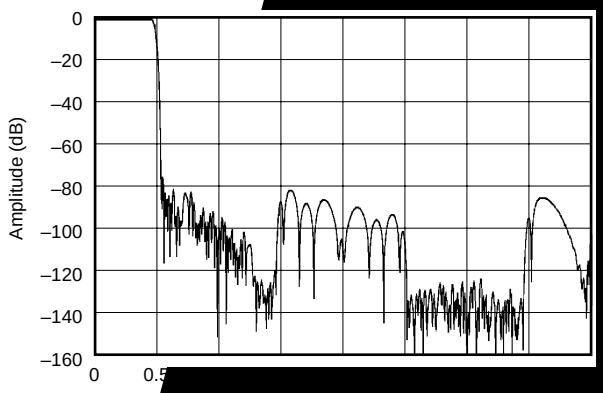


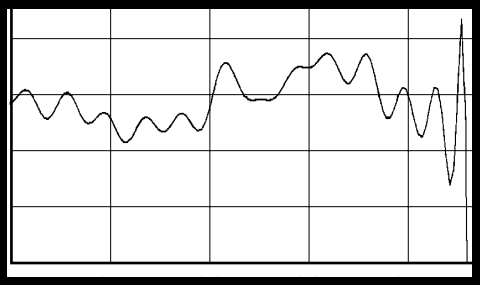
–60dB OUTPUT SPECTRUM
(f = 1kHz, f_S = 44.1kHz, 24-Bit Data)

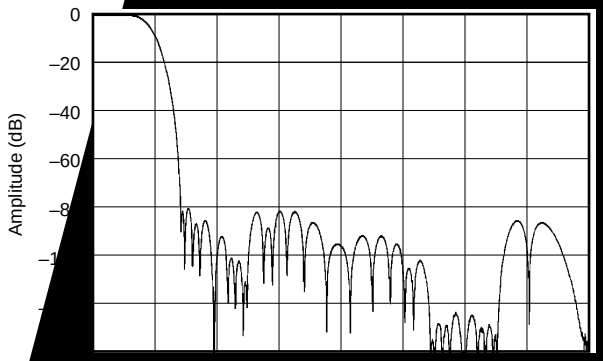


TYPICAL PERFO

OVERALL FR







SYSTEM CLOCK

The system clock for PCM1716 must be either $256f_S$, $384f_S$, $512f_S$ or $768f_S$, where f_S is the audio sampling frequency (typically 32kHz, 44.1kHz, 48kHz, or 96kHz). But $768f_S$ at 96kHz is not accepted.

The system clock can be either a crystal oscillator placed between XTI (pin 5) and XTO (pin 6), or an external clock input to XTI. If an external system clock is used, XTO is open (floating). Figure 1 illustrates the typical system clock connections.

PCM1716 has a system clock detection circuit which automatically senses if the system clock is operating at $256f_S$ ~ $768f_S$. The system clock should be synchronized with LRCIN (pin 1) clock. LRCIN (left-right clock) operates at the sampling frequency f_S. In the event these clocks are not synchronized, PCM1716 can compensate for the phase difference internally. If the phase difference between left-right and system clocks is greater than 6-bit clocks (BCKIN), the synchronization is performed internally. While the synchronization is processing, the analog output is forced to a DC level at bipolar zero. The synchronization typically occurs in less than 1 cycle of LRCIN.

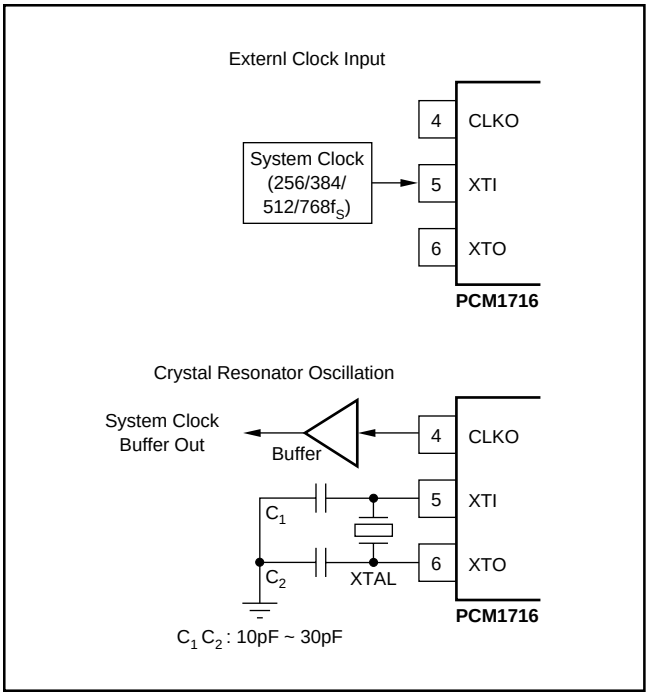


FIGURE 1. System Clock Connection.

Typical input system clock frequencies to the PCM1716 are shown in Table I, also, external input clock timing requirements are shown in Figure 2.

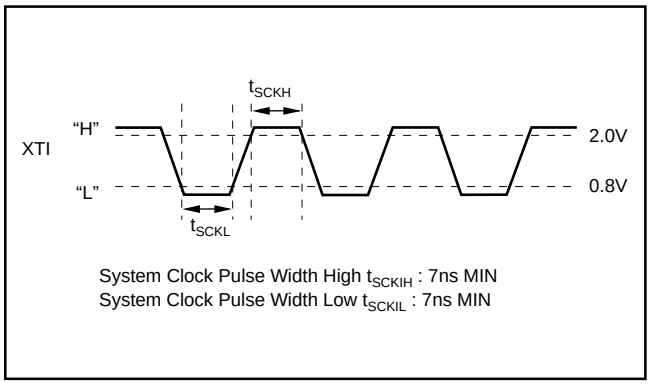


FIGURE 2. XTI Clock Timing.

DATA INTERFACE FORMATS

Digital audio data is interfaced to PCM1716 on pins 1, 2, and 3, LRCIN (left-right clock), DIN (data input) and BCKIN (bit clock). PCM1716 can accept both standard, I^2S, and left justified data formats.

Figure 3 illustrates acceptable input data formats. Figure 4 shows required timing specification for digital audio data.

Reset

PCM1716 has both internal power-on reset circuit and the $\overline{RST}$ pin (pin 22) which accepts an external forced reset by $\overline{RST}$ = LOW. For internal power on reset, initialize (reset) is done automatically at power on V_{DD} >2.2V (typ). During internal reset = LOW, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$. Figure 5 illustrates the timing of the internal power on reset.

PCM1716 accepts an external forced reset when $\overline{RST}$ = L. When $\overline{RST}$ = L, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$ after internal initialization (1024 system clocks count after $\overline{RST}$ = H.) Figure 6 illustrates the timing of the $\overline{RST}$ pin.

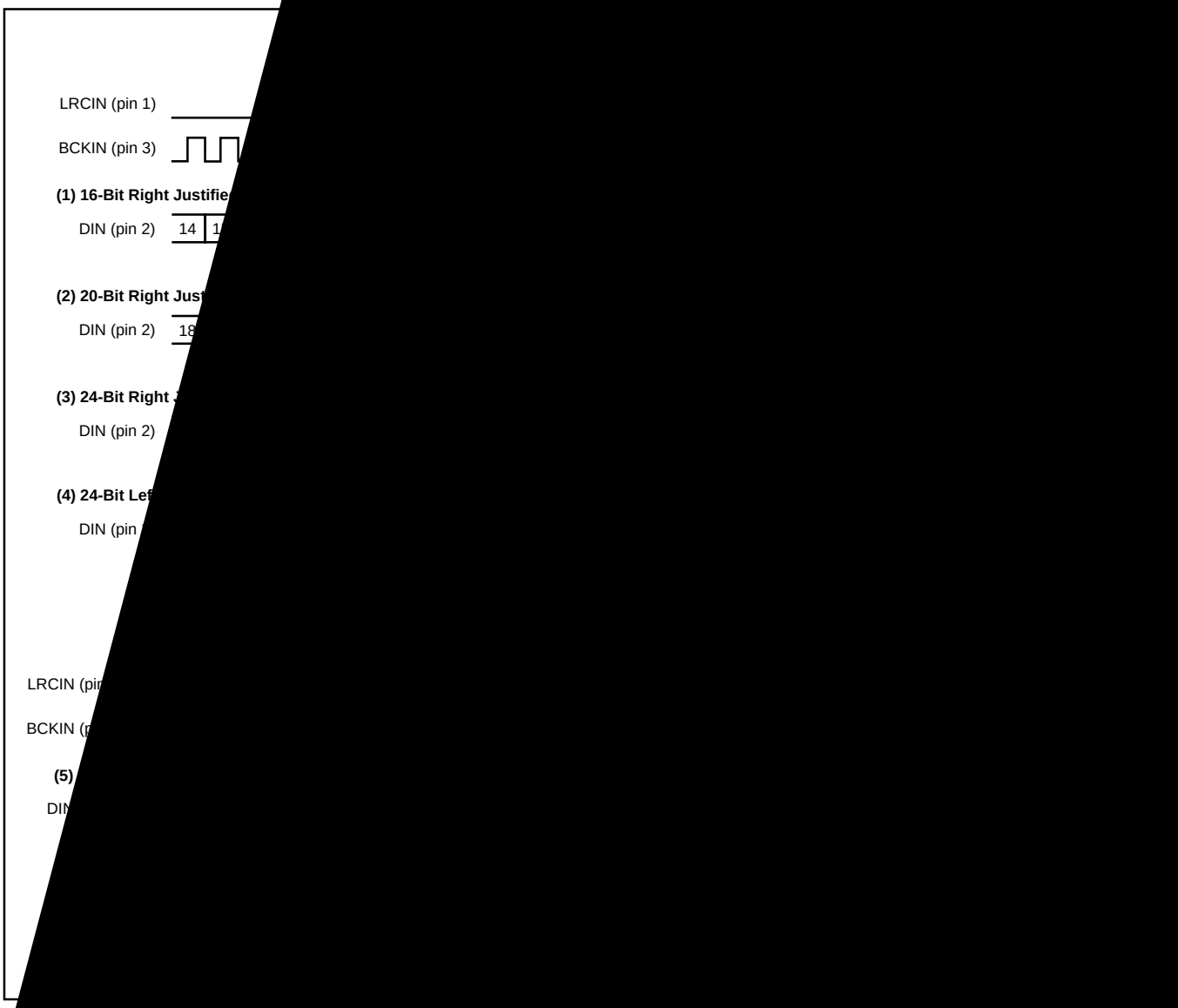
Zero Out (pin 21)

If the input data is continuously zero for 65536 cycles of BCK, an internal FET is switched to "ON". The drain of the internal FET is the zero-pin, it will enable "wired-or" with external circuit. This zero detect function is available in both software mode and hardware mode.

SAMPLING RATE FREQUENCY (f_S) - LRCIN	SYSTEM CLOCK FREQUENCY - MHz			
	$256f_S$	$384f_S$	$512f_S$	$768f_S$
32kHz	8.1920	12.2880	16.3840	24.5760
44.1kHz	11.2896	16.9340	22.5792	33.8688(1)
48kHz	12.2880	18.4320	24.5760	36.8640(1)
96kHz	24.5760	36.8640(1)	49.1520(1)	—

NOTE: (1) The Internal Crystal oscillator frequency cannot be larger than 24.576MHz.

TABLE I. Typical System Clock Frequency.


LRCIN (pin 1)
BCKIN (pin 3)
(1) 16-Bit Right Justifie
DIN (pin 2)
14
(2) 20-Bit Right Just
DIN (pin 2)
18
(3) 24-Bit Right
DIN (pin 2)
(4) 24-Bit Lef
DIN (pin
LRCIN (pi
BCKIN (
(5)
DI

F

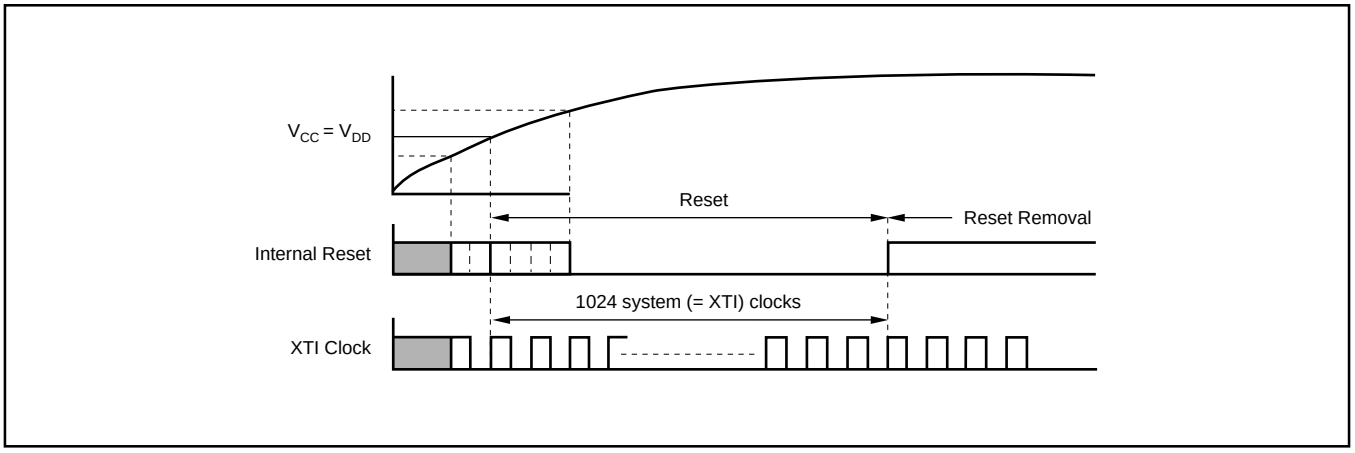


FIGURE 5. Internal Power-On Reset Timing.

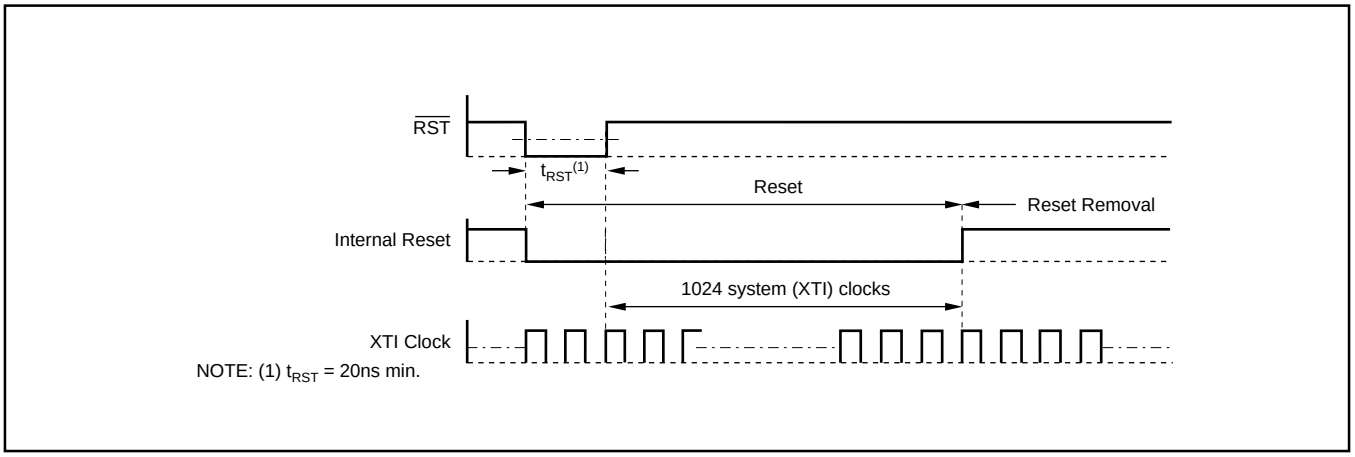


FIGURE 6. External Forced Reset Timing.

FUNCTIONAL DESCRIPTION

PCM1716 has several built-in functions including digital attenuation, digital de-emphasis, input data format selection, and others. These functions are software controlled. PCM1716 can be operated in two different modes, software mode or hardware mode. Software mode is a three-wire interface using pin 28 (ML), 27 (MC), and 26 (MD).

PCM1716 can also be operated in hardware mode, where static control signals are used on pin 28 (115, pin 27 (DM1), pin 26 (DM0) and pin 23 (IWO).

This basic operation mode as software or hardware can be selected by pin 24 (MODE) as shown in Table II.

MODE (pin 24) = H	Software Mode
MODE (pin 24) = L	Hardware Mode

TABLE II. Mode Control.

Table III indicates which functions are selectable within the users chosen mode. All of the functions shown are selectable within the software mode, but only de-emphasis control, soft mute and input data format may be selected when using PCM1716 in the hardware mode.

FUNCTION	SOFTWARE (Mode = H)	HARDWARE (Mode = L)
Input Data Format Selection	O	O
Input Data Bit Selection	O	O
Input LRCIN Polarity Selection	O	X
De-emphasis Control	O	O
Mute	O	O
Attenuation	O	X
Infinity Zero Mute Control	O	X
DAC Operation Control	O	X
Slow Roll-Off Selection	O	X
Output Phase Selection	O	X
CLKO Output Selection	O	X

NOTE: O = Selectable, X: Not Selectable.

TABLE III. Mode Control, Selectable Functions.

HARDWARE MODE (MODE = L)

In hardware mode, the following function can be selected.

De-emphasis control

De-emphasis control can be selected by DM1 (pin 27) and DM0 (pin 26)

DM1 (Pin 27)	DM0 (
L	
L	
H	
H	

TABLE IV. De-emphasis

Input Audio Data Fo

Input data format can
(pin 23)

I²S (Pin 28)	IWO (Pin
L	L
L	H
H	L
H	

TABLE V. Data

SOFT MUTE

Soft Mute fu

M

SOFTW

PCM1
Table
MD

M

REGISTER NAME	BIT NAME	DESCRIPTION
Register 0	AL (7:0) LDL A (1:0) res	DAC Attenuation Data for Lch Attenuation Data Load Control for Lch Register Address Reserved, should be “L”
Register 1	AR (7:0) LDR A (1:0) res	DAC Attenuation Data for Rch Attenuation Data Load Control for Rch Register Address Reserved, should be “L”
Register 2	MUT DEM OPE IW (1:0) res A (1:0) res	Left and Right DACs Soft Mute Control De-emphasis Control Left and Right DACs Operation Control Input Audio Data Bit and Format Select Reserved Register Address Reserved, should be “L”
Register 3	I^2S LRP ATC SRO REV CKO SF (1:0) IZD A (1:0) res	Audio Data Format Select Polarity of LRCIN Select Attenuator Control Slow Roll-Off Select Output Phase Select CLKO Output Select Sampling Rate Select Internal Zero Detection Circuit Control Register Address Reserved, should be “L”

TABLE VII. Register Functions

REGISTER 0 (A1 = 0, A0 = 0)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0

Register 0 is used to control left channel attenuation. Bits 0 - 7 (AL0 - AL7) are used to determine the attenuation level. The level of attenuation is given by:

ATT = 0.5 x (data-255) (dB)
FFh = –0dB
FEh = –0.5dB
:
:
01h = –127.5dB
00h = – ∞ (= Mute)

ATTENUATION DATA LOAD CONTROL

Bit 8 (LDL) is used to control the loading of attenuation data in B0:B7. When LDL is set to 0, attenuation data will be loaded into AL0:AL7, but it will not affect the attenuation level until LDL is set to 1. LDR in Register 1 has the same function for right channel attenuation.

REGISTER 1 (A1 = 0, A0 = 1)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

Register 1 is used to control right channel attenuation. As in Register 1, bits 0 - 7 (AR0 - AR7) control the level of attenuation.

REGISTER 2 (A1 = 1, A0 = 0)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	res	res	res	res	IW1	IWO	OPE	DEM	MUTE

Register 2 is used to control soft mute, de-emphasis, operation enable, input resolution, and input audio data bit and format.

MUT (B0)	
MUT = L	Soft Mute OFF
MUT = H	Soft Mute ON

DEM (B1)	
DEM = L	De-emphasis OFF
DEM = H	De-emphasis ON

OPE (B2)	
OPE = L	Normal Operation
OPE = H	DAC Operation OFF

when OPE (B2) is “HIGH”, the output of the DAC will be forced to bipolar zero, irrespective of any input data.

IWO (B3), IW1 (B4) and I^2S (B0) of Register 3

These resisters, IWO, IW1, I^2S determine the input data word and input data format as shown below.

IW1	IW0	I^2S	Audio Interface
0	0	0	16-Bit Standard (Right-Justified)
0	1	0	20-Bit Standard (Right-Justified)
1	0	0	24-Bit Standard (Right-Justified)
1	1	0	24-Bit Left-Justified (MSB First)
0	0	1	16-Bit I^2S
0	1	1	24-Bit I^2S
1	0	1	Reserved
1	1	1	Reserved

REGISTER 3 (A1 = 1, A0 = 1)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	IZD	SF1	SF0	CKO	REV	SRO	ATC	LRP	I^2S

REGISTER 3 (A1 = 1, A0 = 1)

Register 3 is used to control input data format and polarity, attenuation channel control, system clock frequency, sampling frequency, infinite zero detection, output phase, CLKO output, and slow roll-off.

Bit 8 is used to control the infinite zero detection function (IZD).

When IZD is “LOW”, the zero detect circuit is off. Under this condition, no automatic muting will occur if the input is continuously zero. When IZD is “HIGH”, the zero detect feature is enabled. If the input data is continuously zero for 65, 536 cycles of BCKIN, the output will be immediately

forced to a bipolar zero state
feature is used to avoid noi
input is DC. When the ou
there may be an audible c
detect feature to be disabl
external muting circuit.

IZD (B8)	
B8 = L	
B8 = H	

Bits 6 (SF0) and 7 (
frequency for De-e

SF1	SF0
0	0
0	1
1	0
1	1

CKO (B5) is o
selected as B
(1/2).

CK
Ch

REF (B4

THEORY OF OPERATION

The delta-sigma section of PCM1716 is based on a 8-level amplitude quantizer and a 4th-order noise shaper. This section converts the oversampled input data to 8-level delta-sigma format.

This newly developed, "Enhanced Multi-level Delta-Sigma" architecture achieves high-grade audio dynamic performance and sound quality.

A block diagram of the 8-level delta-sigma modulator is shown in Figure 9. This 8-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8-times interpolation filter is $64f_S$ for all system clock ratios ($256/384/512/768f_S$).

The theoretical quantization noise performance of the 8-level delta-sigma modulator is shown in Figure 10. This enhanced multi-level delta-sigma architecture also has advantages for input clock jitter sensitivity due to the multi-level quantizer, simulated jitter sensitivity is shown in Figure 11.

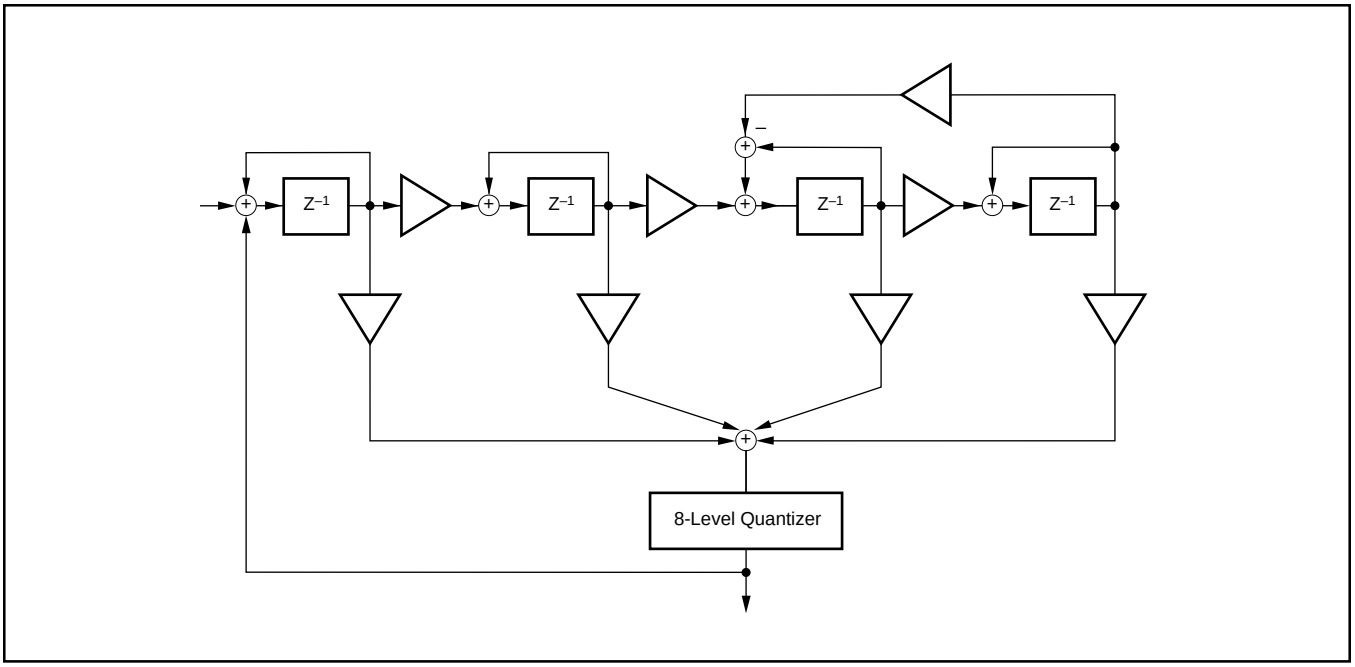


FIGURE 9. 8-Level Delta-Sigma Modulator.

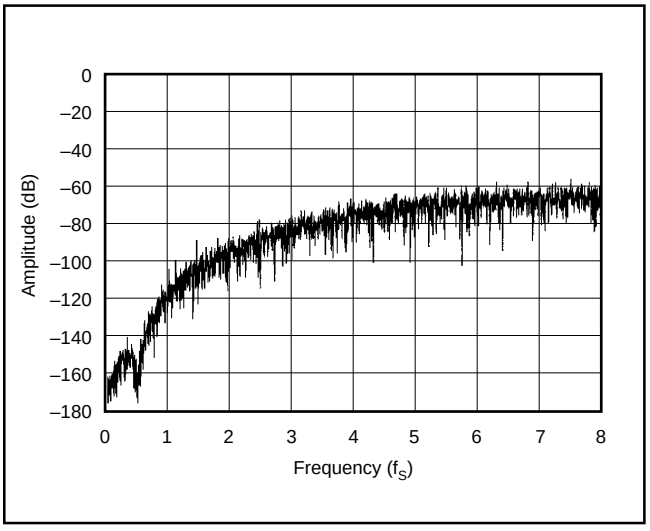


FIGURE 10. Quantization Noise Spectrum.

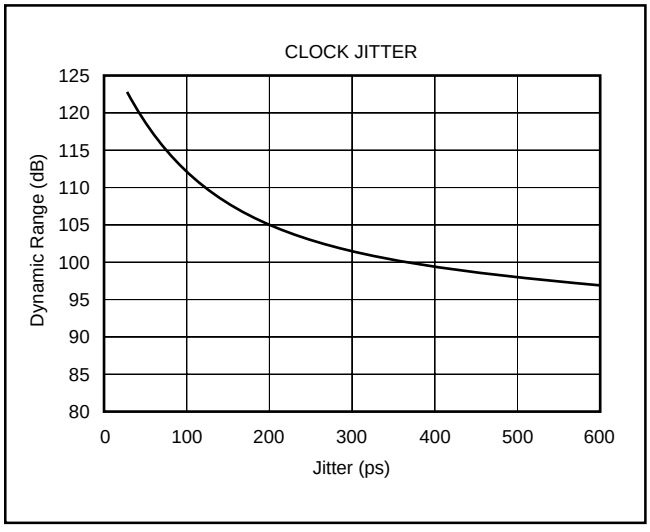


FIGURE 11. Jitter Sensitivity.

APPLICATION CONSIDERATIO

DELAY TIME

There is a finite delay time
converters, this is comm
delta-sigma D/A conver
order number of the FIR
rate. The following e
PCM1716:

For f_S = 44.

Applications usin
CD audio, DVD
generally are no
sional applicati
important for t

OUTPUT F

For testing
PCM1716
the measu
to use suc
SNR and
specifica
noise.
specifi

The p
40kH
of t
has
me

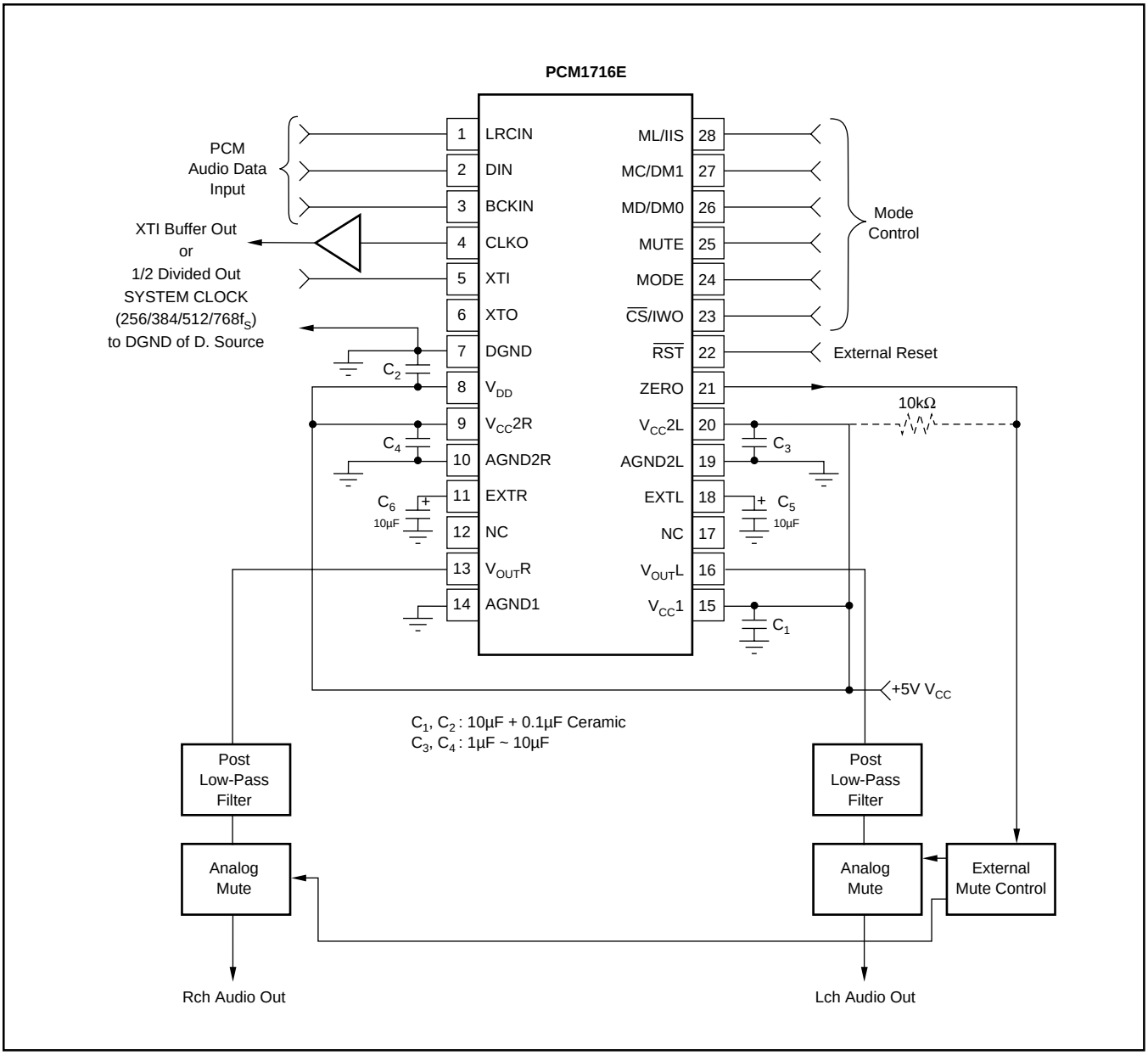


FIGURE 15. Typical Circuit Connection Diagram.

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
PCM1716E	ACTIVE	SSOP	DB	28	47
PCM1716E/2K	ACTIVE	SSOP	DB	28	2000

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automo.4(aio)]0	