Ordering number : EN 5121B

CMOS LSI

LC78630E

Compact Disk Player DSP

Overview

The LC78630E is a CD-DA signal-processing LSI for use in video CD player systems. The LC78630E incorporates signal-processing circuits for demodulating and de-interleaving the EFM signal from the optical pickup, error detection and correction, and digital filtering. It also includes a 1-bit D/A converter and executes commands sent from a system control microprocessor.

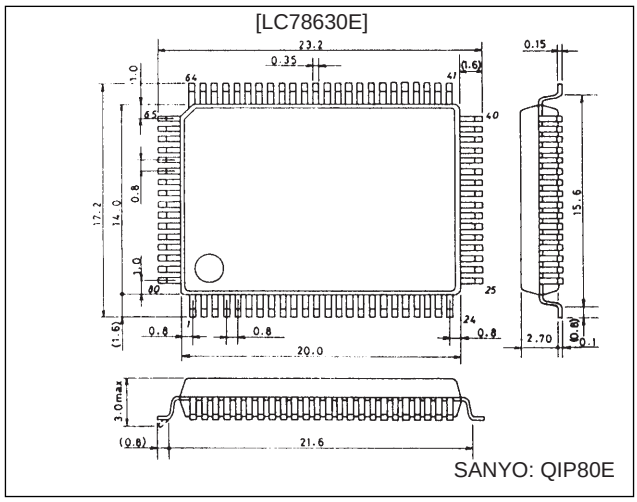
Features

- Built-in PLL for EFM signal synchronization (a hybrid analog-digital PLL that supports 4× playback)
- Built-in PLL for variable pitch playback (±13%)
- 18KB RAM on chip
- Error detection and correction (corrects two errors in C1 and four errors in C2)
- Frame jitter margin: ±8 frames
- Frame synchronization signal detection, protection, and insertion
- Dual interpolation adopted in the interpolation circuit.
- EFM data demodulation
- Subcode demodulation
- Zero-cross muting adopted
- Servo command interface
- 2fs digital filter
- Digital de-emphasis
- Built-in independent left- and right-channel digital attenuators (239 attenuation steps)
- Left/right swap function
- Built-in 1-bit D/A converter (third-order ΔΣ noise shaper, PWM output)
- Built-in digital output circuit
- CLV servo
- Arbitrary track jumping (of up to 255 tracks)
- Variable sled voltage (four levels)
- Built-in oscillator circuit using an external 16.9344 MHz or 33.8688 MHz (for 4× playback) element
- Supply voltage: 3.6 to 5.5 V (4.5 to 5.5 V for 4× playback mode)
- Six extended I/O ports and 2 extended output ports

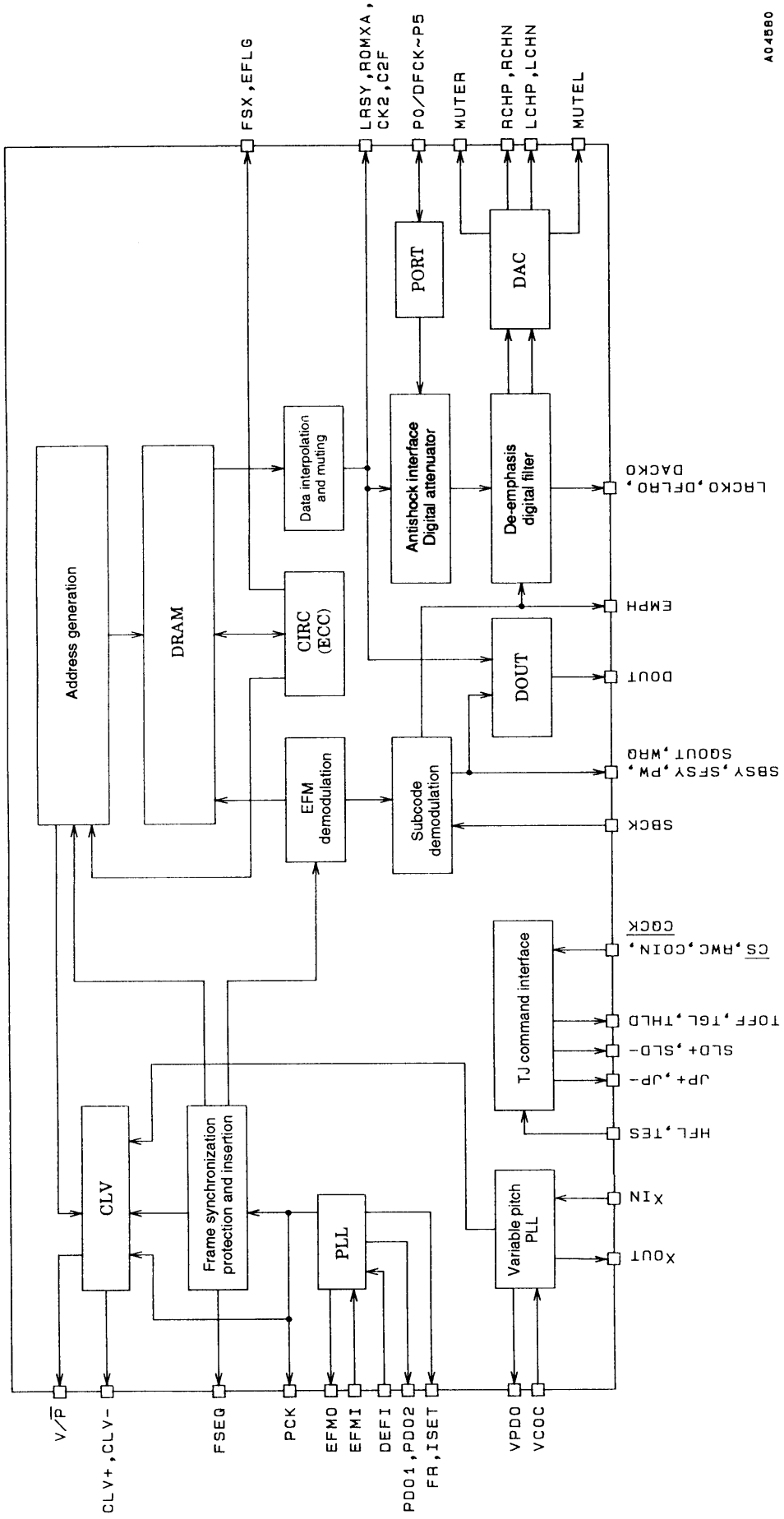
Package Dimensions

unit: mm

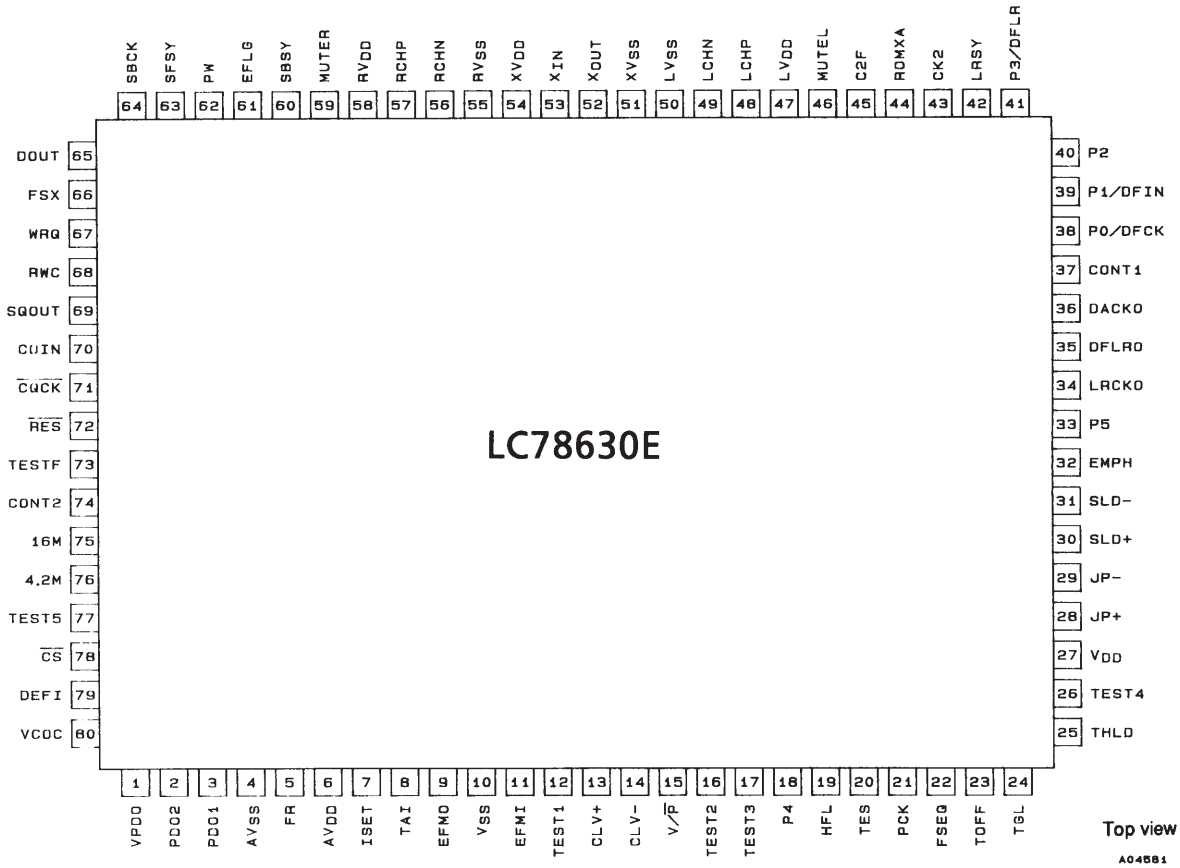
3174-QFP80E



Equivalent Circuit Block Diagram



Pin Assignment



Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Input voltage	V_{IN}		–0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}		–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max		470	mW
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD}1$	V_{DD}, AV_{DD}, XV_{DD}, LV_{DD}, RV_{DD}	3.6	5.0	5.5	V
	$V_{DD}2$	V_{DD}, AV_{DD}, XV_{DD}, LV_{DD}, RV_{DD}: For 4× playback or variable-pitch playback	4.5	5.0	5.5	V
Input high-level voltage	$V_{IH}1$	TEST1 to TEST5, TAI, HFL, TES, P0/DFCK, P1/DFIN, P2, P3/DFLR, P4, P5, SBCK, RWC, COIN, $\overline{CQCK}$, $\overline{RES}$, $\overline{CS}$, X_{IN}, DEFI	0.7 V_{DD}		V_{DD}	V
	$V_{IH}2$	EFMI	0.6 V_{DD}		V_{DD}	V
Input low-level voltage	$V_{IL}1$	TEST1 to TEST5, TAI, HFL, TES, P0/DFCK, P1/DFIN, P2, P3/DFLR, P4, P5, SBCK, RWC, COIN, $\overline{CQCK}$, $\overline{RES}$, $\overline{CS}$, X_{IN}, DEFI	0		0.3 V_{DD}	V
	$V_{IL}2$	EFMI	0		0.4 V_{DD}	V
Data setup time	t_{SU}	COIN, RWC: Figures 1 and 4	400			ns
	t_{PRS}	RWC: Figure 4	100			ns
Data hold time	t_{HD}	COIN, RWC: Figures 1 and 4	400			ns

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Parameter	Symbol	Conditions	min	typ	max	Unit
High-level clock pulse width	t_{WH}	SBCK, $\overline{CQCK}$: Figures 1, 2, 3, and 4	400			ns
Low-level clock pulse width	t_{WL}	SBCK, $\overline{CQCK}$: Figures 1, 2, 3, and 4	400			ns
Data read access time	t_{RAC}	SQOUT, PW: Figures 2, 3, and 4	0		400	ns
Command transfer time	t_{RWC}	RWC: Figures 1 and 4	1000			ns
Subcode Q read enable time	t_{SQE}	WRQ: Figure 2, with no RWC signal		11.2		ms
Subcode read cycle	t_{SC}	SFSY: Figure 3		136		µs
Subcode read enable	t_{SE}	SFSY: Figure 3	400			ns
Port output delay time	t_{PD}	CONT1, CONT2, P0 to P5: Figure 5			1200	ns
Input level	V_{EI}	EFMI	1.0			Vp-p
	V_{XI}	X_{IN}: Capacitance coupled input	1.0			Vp-p

Note: Due to the structure of this IC, the identical voltage must be applied to all power-supply pins.

Electrical Characteristics at Ta = 25°C, V_{DD} = 5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	I_{DD}			30		mA
Input high-level current	$I_{IH}1$	EFMI, HFL, TES, SBCK, RWC, COIN, $\overline{CQCK}$, $\overline{RES}$, DEFI: V_{IN} = 5 V			5	µA
	$I_{IH}2$	TAI, TEST1 to TEST5, CS: V_{IN} = 5 V	25		75	µA
Input low-level current	I_{IL}	TAI, EFMI, HFL, TES, SBCK, RWC, COIN, $\overline{CQCK}$, $\overline{RES}$, TEST1 to TEST5, CS, DEFI: V_{IN} = 0 V	–5			µA
Output high-level voltage	$V_{OH}1$	EFMO, CLV^+, CLV^-, V/P, PCK, FSEQ, TOFF, TGL, THLD, JP^+, JP^-, EMPH, EFLG, FSX: I_{OH} = –1 mA	4			V
	$V_{OH}2$	MUTEL, MUTER, LRCKO, DFLRO, DACKO, P0/DFCK, P1/DFIN, P2, P3/DFLR, P4, P5, LRSY, CK2, ROMXA, C2F, SBSY, PW, SFSY, WRQ, SQOUT, 16M, 4.2M, CONT1, CONT2: I_{OH} = –0.5 mA	4			V
	$V_{OH}3$	VPDO: I_{OH} = –1 mA	4.5			V
	$V_{OH}4$	DOUT: I_{OH} = –12 mA	4.5			V
	$V_{OH}5$	LCHP, RCHP, LCHN, RCHN: I_{OH} = –1 mA	3.0		4.5	V
Output low-level voltage	$V_{OL}1$	EFMO, CLV^+, CLV^-, V/P, PCK, FSEQ, TOFF, TGL, THLD, JP^+, JP^-, EMPH, EFLG, FSX: I_{OL} = 1 mA			1	V
	$V_{OL}2$	MUTEL, MUTER, LRCKO, DFLRO, DACKO, P0/DFCK, P1/DFIN, P2, P3/DFLR, P4, P5, LRSY, CK2, ROMXA, C2F, SBSY, PW, SFSY, WRQ, SQOUT, 16M, 4.2M, CONT1, CONT2: I_{OL} = 2 mA			0.4	V
	$V_{OL}3$	VPDO: I_{OL} = 1 mA			0.5	V
	$V_{OL}4$	DOUT: I_{OL} = 12 mA			0.5	V
	$V_{OL}5$	LCHP, RCHP, LCHN, RCHN: I_{OL} = 1 mA	0.5		2.0	V
Output off leakage current	$I_{OFF}1$	PDO1, PDO2, VPDO, P0/DFCK, P1/DFIN, P2, P3/DFLR, P4, P5: V_{OUT} = 5 V			5	µA
	$I_{OFF}2$	PDO1, PDO2, VPDO, P0/DFCK, P1/DFIN, P2, P3/DFLR, P4, P5: V_{OUT} = 0 V	–5			µA
Charge pump output current	I_{PDOH}	PDO1, PDO2: R_{ISET} = 68 kΩ	–96	–80	–64	µA
	I_{PDOL}	PDO1, PDO2: R_{ISET} = 68 kΩ	64	80	96	µA
Sled output voltage	$V_{SLD}1$		1.0	1.25	1.5	V
	$V_{SLD}2$		2.25	2.5	2.75	V
	$V_{SLD}3$		3.5	3.75	4.0	V
	$V_{SLD}4$		4.75			V

D/A Converter Analog Characteristics at Ta = 25°C, V_{DD} = 5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Total harmonic distortion	THD + N	LCHP, LCHN, RCHP, RCHN; 1 kHz: 0 dB input, using a 20-kHz low-pass filter (AD725D built in)		0.006		%
Dynamic range	DR	LCHP, LCHN, RCHP, RCHN; 1 kHz: –60 dB input, using the 20-kHz low-pass filter (A filter (AD725D built in))		90		dB
Signal-to-noise ratio	S/N	LCHP, LCHN, RCHP, RCHN; 1 kHz: 0 dB input, using the 20-kHz low-pass filter (A filter (AD725D built in))	98	100		dB
Crosstalk	CT	LCHP, LCHN, RCHP, RCHN; 1 kHz: 0 dB input, using a 20-kHz low-pass filter (AD725D built in)	96	98		dB

Note: Measured in normal-speed playback mode in a Sanyo 1-bit D/A converter block reference circuit, with the digital attenuator set to EE`p (hexadecimal).

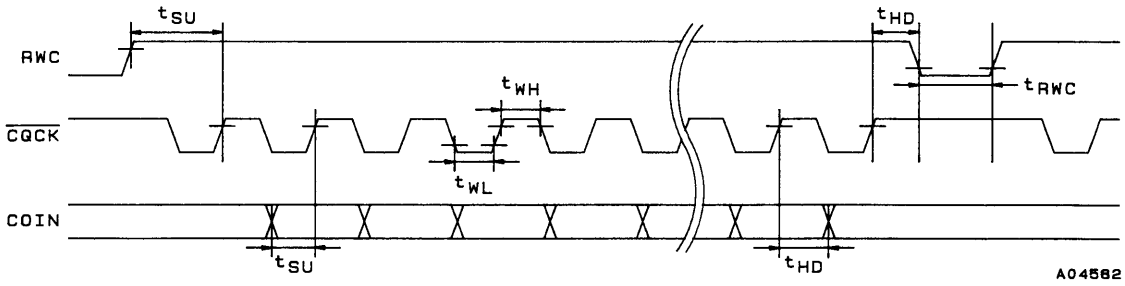


Figure 1 Command Input

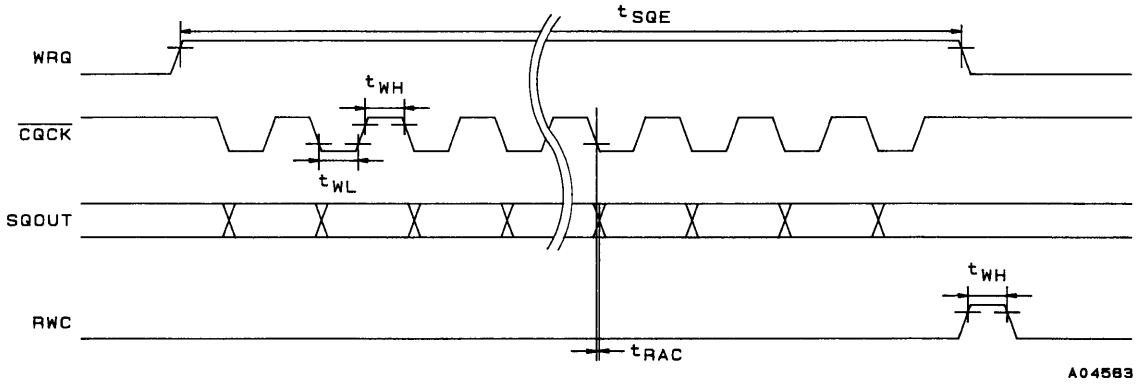


Figure 2 Subcode Q Output

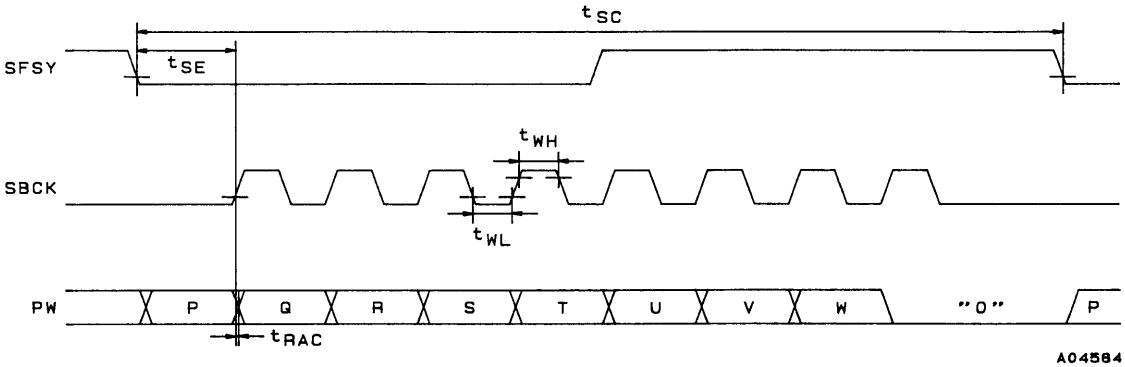


Figure 3 Subcode Output

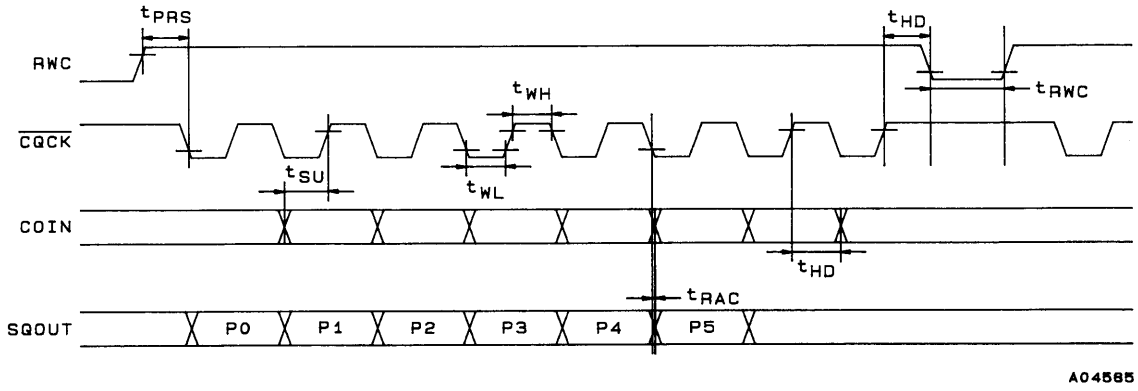


Figure 4 General-Purpose Port Read

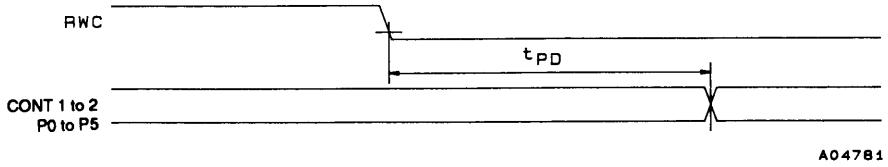
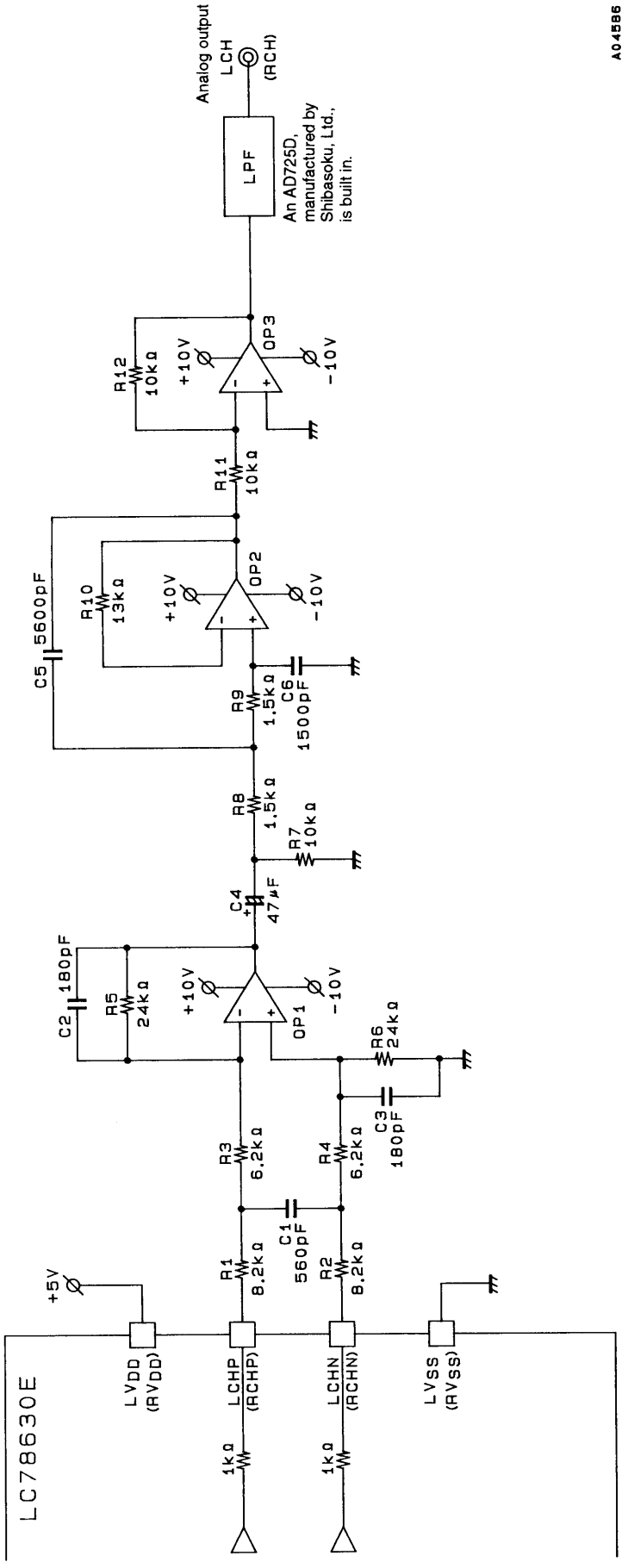


Figure 5 General-Purpose Port Output

One-Bit D/A Converter Output Block Reference Circuit



Pin Functions

Pin No.	Symbol	I/O	Function	
1	VPDO	O	Variable pitch PLL charge pump output. Must be left open if unused.	
2	PDO2	O	Double-speed and quad-speed mode playback PLL charge pump output. Must be left open if unused.	
3	PDO1	O	Normal-speed mode playback PLL charge pump output	
4	AV_{SS}		Analog system ground. Normally 0 V.	
5	FR		Built-in VCO frequency range setting resistor connection	
6	AV_{DD}		Analog system power supply.	
7	ISET		PDO1 and PDO2 output current setting resistor connection	
8	TAI	I	Test input. A pull-down resistor is built in.	
9	EFMO	O	EFM signal output	
10	V_{SS}		Digital system ground. Normally 0 V.	
11	EFMI	I	EFM signal input	
12	TEST1	I	Test input. A pull-down resistor is built in.	
13	CLV^+	O	Spindle servo control output. CLV^+ outputs a high level for acceleration, and CLV^- outputs a high level for deceleration.	
14	CLV^-	O		
15	$V/\overline{P}$	O	Rough servo/phase control automatic switching monitor output. A high-level output indicates rough servo, and a low-level output indicates phase control.	
16	TEST2	I	Test input. A pull-down resistor is built in.	
17	TEST3	I	Test input. A pull-down resistor is built in.	
18	P4	I/O	I/O port	
19	HFL	I	Track detection signal input. This is a Schmitt input.	
20	TES	I	Tracking error signal input. This is a Schmitt input.	
21	PCK	O	EFM data playback bit clock monitor. Outputs 4.3218 MHz when the phase is locked in normal-speed mode playback.	
22	FSEQ	O	Synchronization signal detection output. Outputs a high level when the synchronization signal detected from the EFM signal matches the internally generated synchronization signal.	
23	TOFF	O	Tracking off output	
24	TGL	O	Tracking gain switching output. Increase the gain when this pin outputs a low level.	
25	THLD	O	Tracking hold output.	
26	TEST4	I	Test input. A pull-down resistor is built in.	
27	V_{DD}		Digital system power supply.	
28	JP^+	O	Track jump output. JP^+ outputs a high level both for acceleration during outward direction jumps and for deceleration during inward direction jumps. JP^- outputs a high level both for acceleration during inward direction jumps and for deceleration during outward direction jumps.	
29	JP^-	O		
30	SLD^+	O	Sled output. This pin can be set to 1 of 4 levels by commands sent from the system control microprocessor.	
31	SLD^-	O		
32	EMPH	O	De-emphasis monitor. A high level indicates that a disk requiring de-emphasis is being played.	
33	P5	I/O	I/O port	
34	LRCKO	O	Digital filter outputs	LR clock output
35	DFLRO	O		LR data output. The digital filter can be turned off with the DFOFF command.
36	DACKO	O		Bit clock output
37	CONT1	O	Output port	
38	P0/DFCK	I/O	I/O port or digital filter bit clock input	
39	P1/DFIN	I/O	I/O port or digital filter data input	
40	P2	I/O	I/O port. Used as the de-emphasis filter on/off switching pin in antishock mode. The de-emphasis filter is turned on when this pin is high.	
41	P3/DFLR	I/O	I/O port output or digital filter LR clock input (when anti-shock mode)	
42	LRSY	O	ROMXA pins	LR clock output
43	CK2	O		Bit clock output. The polarity can be inverted with the CK2CON command.
44	ROMXA	O		Interpolated data output. Data that has not been interpolated can be output by issuing the ROMXA command.
45	C2F	O		C2 flag output
46	MUTEL	O	One-bit D/A converter pins	Left channel mute output
47	LV_{DD}			Left channel power supply.
48	LCHP	O		Left channel P output
49	LCHN	O		Left channel N output
50	LV_{SS}			Left channel ground. Normally 0 V.

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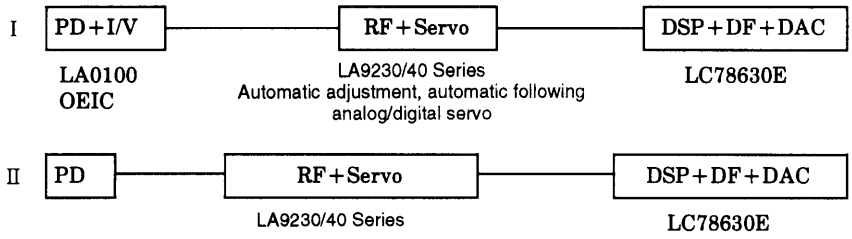
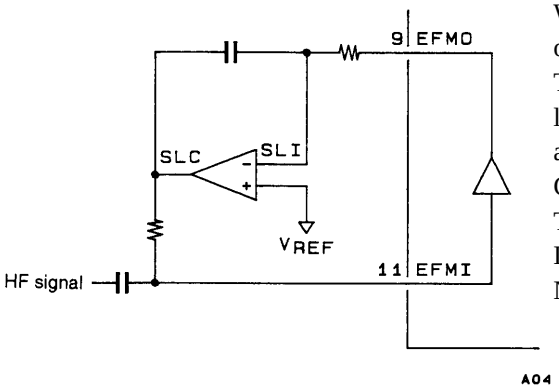
Pin No.	Symbol	I/O	Function	
51	XV_{SS}		Crystal oscillator ground. Normally 0 V.	
52	X_{OUT}	O	16.9344 MHz crystal oscillator connections. Use a 33.8688 MHz crystal oscillator for quad-speed playback.	
53	X_{IN}	I		
54	XV_{DD}		Crystal oscillator power supply.	
55	RV_{SS}		One-bit D/A converter pins	Right channel ground. Normally 0 V.
56	RCHN	O		Right channel N output
57	RCHP	O		Right channel P output
58	RV_{DD}			Right channel power supply.
59	MUTER	O		Right channel mute output
60	SBSY	O	Subcode block synchronization signal output	
61	EFLG	O	C1 and C2 error correction state monitor	
62	PW	O	Subcode P, Q, R, S, T, U, V, and W output	
63	SFSY	O	Subcode frame synchronization signal output. Falls when the subcode output goes to the standby state.	
64	SBCK	I	Subcode readout clock input. This is a Schmitt input.	
65	DOUT	O	Digital output	
66	FSX	O	Outputs a 7.35 kHz synchronization signal generated by dividing the crystal oscillator frequency.	
67	WRQ	O	Subcode Q output standby output	
68	RWC	I	Read/write control input	
69	SQOUT	O	Subcode Q output	
70	COIN	I	Input for commands from the control microprocessor	
71	$\overline{CQCK}$	I	Command input acquisition clock. Also used as the SQOUT subcode readout clock input. This is a Schmitt input.	
72	$\overline{RES}$	I	Chip reset input. This pin must be set low temporarily when power is first applied.	
73	TESTF	O	Test output	
74	CONT2	O	Output port	
75	16M	O	16.9344 MHz output. 33.8688 MHz output in 4 × playback mode	
76	4.2M	O	4.2336 MHz output	
77	TEST5	I	Test input. A pull-down resistor is built in.	
78	CS	I	Chip select input. A pull-down resistor is built in. Must be connected to ground if unused.	
79	DEFI	I	Defect detection signal input. Must be connected to ground if unused.	
80	VCOC	I	Variable pitch VCO control input. Must be connected to ground if unused.	

CD D/A Converter Block Diagram



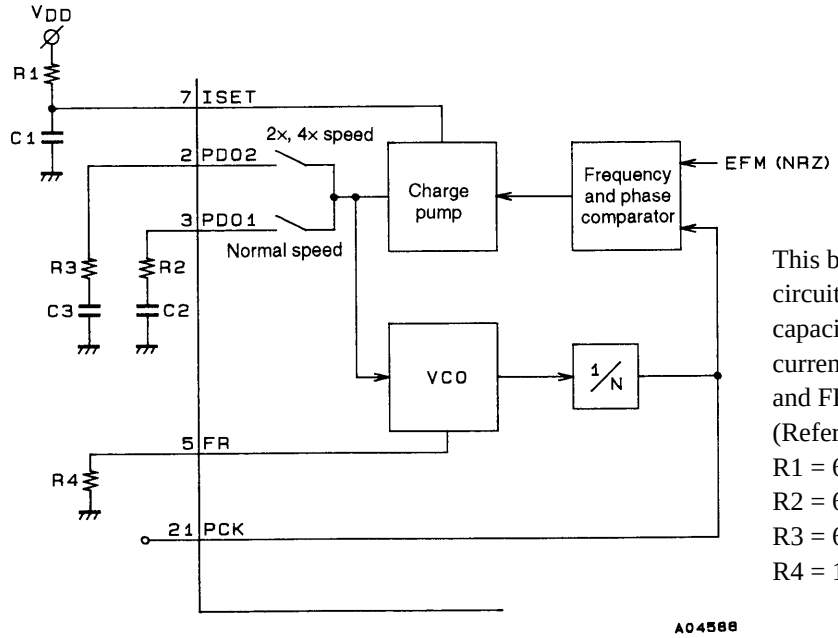
1. HF signal input circuit; Pin 11: EFMI, pin 9: EFMO, pin 79: DEFI, pin 13: CLV+



When an HF signal is input to EFMI, the circuit slices it at an optimal level to produce an EFM (NRZ) signal.
To deal with defects, if the DEFI pin (pin 79) goes high, the slice level control output (EFMO, pin 9) goes to the high-impedance state and the slice level is held. However, this function only operates when CLV is in phase control mode, i.e., when the V/P pin (pin 15) is low. This function can be formed by combining with the DEF pin on the LA9230/40 Series LSI.

Note: If the EFMI and CLV+ lines are placed too close together, spurious radiation (induced noise) can degrade the error rate. Therefore we recommend laying a ground or V_{DD} shielding line between these lines.

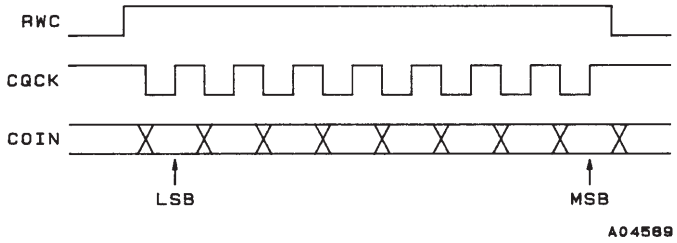
2. PLL clock reproduction circuit; Pin 2: PDO2, pin 3: PDO1, pin 5: FR, pin 7: ISET, pin 21: PCK



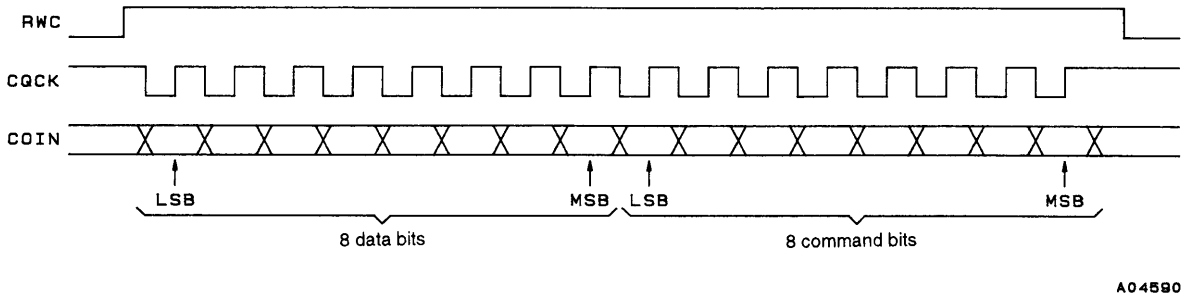
This block includes a VCO circuit, and a PLL circuit is formed using external resistors and capacitors. ISET is the charge pump reference current, PDO1 and PDO2 are the loop filters, and FR determines the VCO frequency range. (Reference values)
R1 = 68 kΩ, C1 = 0.1 µF
R2 = 680 Ω, C2 = 0.1 µF
R3 = 680 Ω, C3 = 0.047 µF
R4 = 1.2 kΩ

3. Synchronization detection monitor; Pin 22: FSEQ
This pin outputs a high level when the frame sync (positive synchronizing signal), which is read by PCK from the EFM signal, and the timing (the inserted synchronizing signal), which is generated by a counter, agree. Thus this pin functions as a synchronization monitor. Note that it is held high during one frame.

4. Command input
   An external controller can execute LC78630E instructions by setting RWC high and inputting commands to COIN in synchronization with the $\overline{\text{CQCK}}$ clock. Commands are executed on the fall of the RWC signal.
   • Single-byte commands



   • Two-byte commands



   • Command noise reduction

Code	Command	$\overline{\text{RES}}$ = low
$EF	COMMAND INPUT NOISE REDUCTION MODE	
$EE	CLEAR THE ABOVE MODE	❍

   This command can reduce the noise on the $\overline{\text{CQCK}}$ clock signal. While this is effective for noise pulses under 500 ns, the use of this function requires that the $\overline{\text{CQCK}}$ timings t_{WL}, t_{WH}, and t_{SU} (see Figure 1 and 2) be set to 1 µs or longer.

5. CLV servo circuit
   • CLV servo circuit; Pin 13: CLV^+, pin 14: CLV^-, pin 15: $V/\overline{P}$

Code	Command	$\overline{\text{RES}}$ = low
$04	DISC MOTOR START (accelerate)	
$05	DISC MOTOR CLV (CLV)	
$06	DISC MOTOR BRAKE (decelerate)	
$07	DISC MOTOR STOP (stop)	❍

   The CLV^+ signal causes the disc to accelerate in the forward direction, and CLV^- causes the disc to decelerate. The microcontroller can select one of four modes: accelerate, decelerate, CLV, and stop. The table below lists the states of the CLV^+ and CLV^- pins in each of these modes.

Mode	CLV^+	CLV^-
Accelerate	High	Low
Decelerate	Low	High
CLV	Pulse output	Pulse output
Stop	Low	Low

   Note: The CLV servo control commands only set the TOFF pin low during CLV mode. That pin will be at the high level at all other times. Thus controlling the TOFF pin with microcontroller commands is only possible in CLV mode.

• CLV mode

In CLV mode, the system detects the disc speed from the HF signal and holds the disc at the prescribed linear speed using multiple control methods switched by changing the DSP internal mode. The PWM frequency is 7.35 kHz. The V/$\overline{P}$ pin outputs a high level when the system is in rough servo mode and a low level when it is in phase control mode.

Internal mode	CLV+	CLV−	V/$\overline{P}$
Rough servo (velocity too low)	High	Low	High
Rough servo (velocity too high)	Low	High	High
Phase control (PCK locked)	PWM	PWM	Low

• Rough servo gain switching

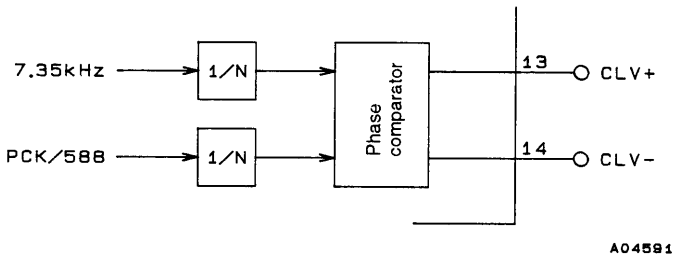
Code	Command	$\overline{RES}$ = low
$A8	8-cm DISC LOADED	
$A9	12-cm DISC LOADED	❍

The CLV control gain in rough servo mode can be reduced by 8.5 dB from the 12-cm disc setting for 8-cm discs.

• Phase control gain switching

Code	Command	$\overline{RES}$ = low
$B1	CLV PHASE COMPARATOR DIVISOR: 1/2	
$B2	CLV PHASE COMPARATOR DIVISOR: 1/4	
$B3	CLV PHASE COMPARATOR DIVISOR: 1/8	
$B0	NO CLV PHASE COMPARATOR DIVISOR USED	❍

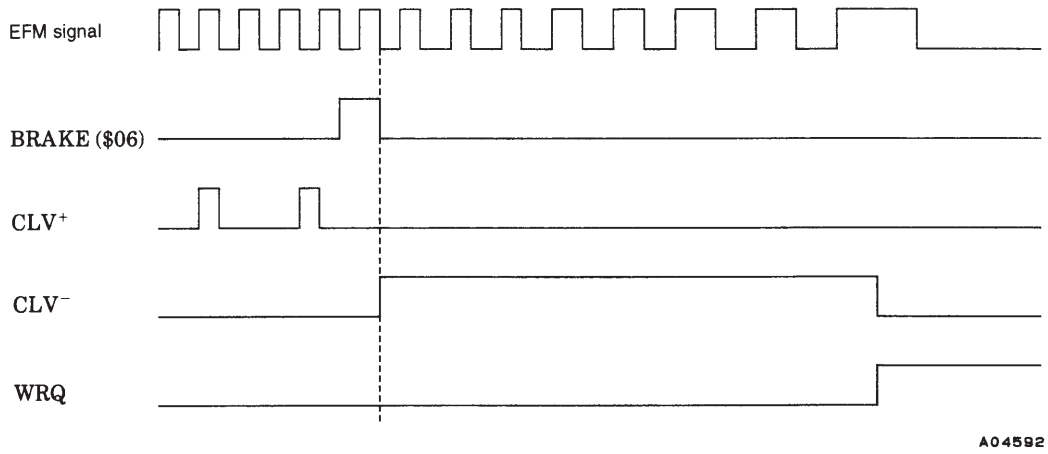
The phase control gain can be switched by switching the value of the divisor in the dividers in the stage preceding the phase comparator.



• Internal brake modes

Code	Command	$\overline{RES}$ = low
$C5	INTERNAL BRAKE ON	
$C4	INTERNAL BRAKE OFF	❍
$A3	INTERNAL BRAKE CONT	
$CB	INTERNAL BRAKE CONTINUOUS MODE	
$CA	RESET CONTINUOUS MODE	❍
$CD	TON MODE DURING INTERNAL BRAKING	
$CC	RESET TON MODE	❍

— Inputting the internal brake on command ($C5) sets the system to internal braking mode. In this mode, executing a brake command ($06) allows the disc deceleration state to be monitored from the WRQ pin.
— In this mode the system counts the density of the EFM signal during one frame to determine the disk deceleration state and drops CLV⁻ to low when the EFM signal falls to 4 or lower. At this point, it sets the WRQ signal high as a braking complete monitor. When the microcontroller detects a high level on the WRQ signal, it should issue a STOP command to completely stop the disc. In internal braking continuous mode ($CB), the LSI continues the braking operation by holding CLV⁻ high even after the WRQ braking done monitor signal has been set high.
Note that there are cases where, to compensate for incorrect braking state recognition due to noise in the EFM signal, the EFM signal count should be changed from 4 to 8 using the internal brake control command ($A3).
— In TON mode during internal braking ($CD), the TOFF signal is set low during internal braking operation. We recommend using this mode, since it is effective at preventing incorrect detection at the disk mirror surface.



Note: 1. If focus is lost during the execution of an internal braking command, the pickup must be refocussed and the internal braking command must be input once again.
2. Since incorrect judgments are possible due to the EFM signal reproduction state (due damaged disks, access in progress, and other problems), we recommend using a microcontroller in conjunction with this LSI.

6. Track jump
• Track jump circuit; Pin 19: HFL, pin 20: TES, pin 23: TOFF, pin 24: TGL, pin 25: THLD, pin 28: JP⁺, pin 29: JP⁻

Code	Command	$\overline{RES}$ = low
$22	NEW TRACK COUNT (using the TES/HFL combination)	○
$23	OLD TRACK COUNT (directly counts the TES signal)	

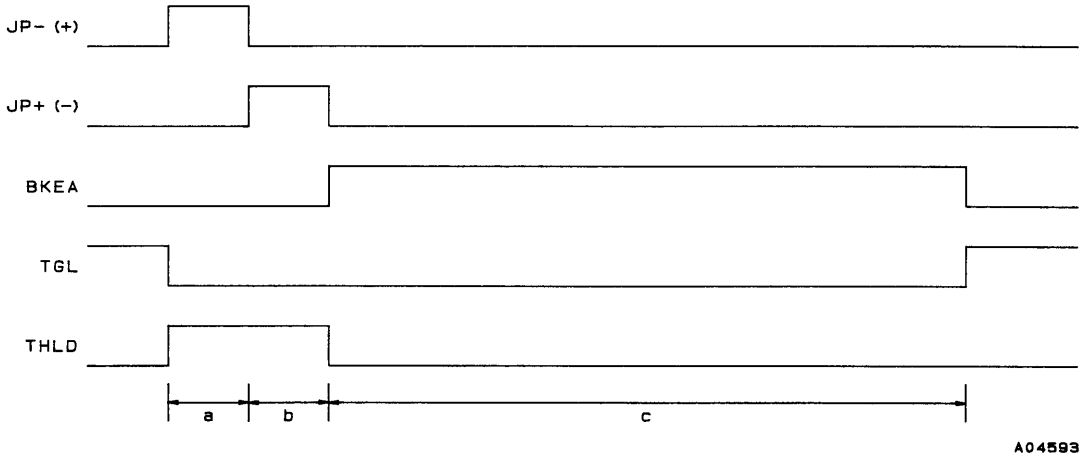
The LC78630E supports the two track count modes listed below.
The old track count function uses the TES signal directly as the internal track counter clock.
To reduce counting errors resulting from noise on the rising and falling edges of the TES signal, the new track count function prevents noise induced errors by using the combination of the TES and HFL signals, and implements a more reliable track count function. However, dirt and scratches on the disk can result in HFL signal dropouts that may result in missing track count pulses. Thus care is required when using this function.

Code	Command	$\overline{RES}$ = low
$BA	TES WD WIDE	○
$BB	TES WD NARW	

The new track jump mode applies a window to the TES and HFL signals. The LC78630E provides two widths for this window.
TES WD WIDE.....The maximum input frequency for TES and HFL is 60 kHz.
TES WD NARW .....The maximum input frequency for TES and HFL is 120 kHz.

• TJ commands

Code	Command	$\overline{RES}$ = low
$A0	OLD TRACK JUMP	○
$A1	NEW TRACK JUMP	
$11	1 TRACK JUMP IN #1	
$12	1 TRACK JUMP IN #2	
$31	1 TRACK JUMP IN #3	
$52	1 TRACK JUMP IN #4	
$10	2 TRACK JUMP IN	
$13	4 TRACK JUMP IN	
$14	16 TRACK JUMP IN	
$30	32 TRACK JUMP IN	
$15	64 TRACK JUMP IN	
$17	128 TRACK JUMP IN	
$19	1 TRACK JUMP OUT #1	
$1A	1 TRACK JUMP OUT #2	
$39	1 TRACK JUMP OUT #3	
$5A	1 TRACK JUMP OUT #4	
$18	2 TRACK JUMP OUT	
$1B	4 TRACK JUMP OUT	
$1C	16 TRACK JUMP OUT	
$38	32 TRACK JUMP OUT	
$1D	64 TRACK JUMP OUT	
$1F	128 TRACK JUMP OUT	
$16	256 TRACK CHECK	
$0F	TOFF	
$8F	TON	○
$8C	TRACK JUMP BRAKE	
$21	THLD PERIOD TOFF OUTPUT MODE	



When the LC78630E receives a track jump instruction as a servo command, it first generates accelerating pulses (period a) and next generates deceleration pulses (period b). The passage of the braking period (period c) completes the specified jump. During the braking period, the LC78630E detects the beam slip direction from the TES and HFL inputs. TOFF is used to cut the components in the TES signal that aggravate slip. The jump destination track is captured by increasing the servo gain with TGL. In THLD period TOFF output mode the TOFF signal is held high during the period when THLD is high.

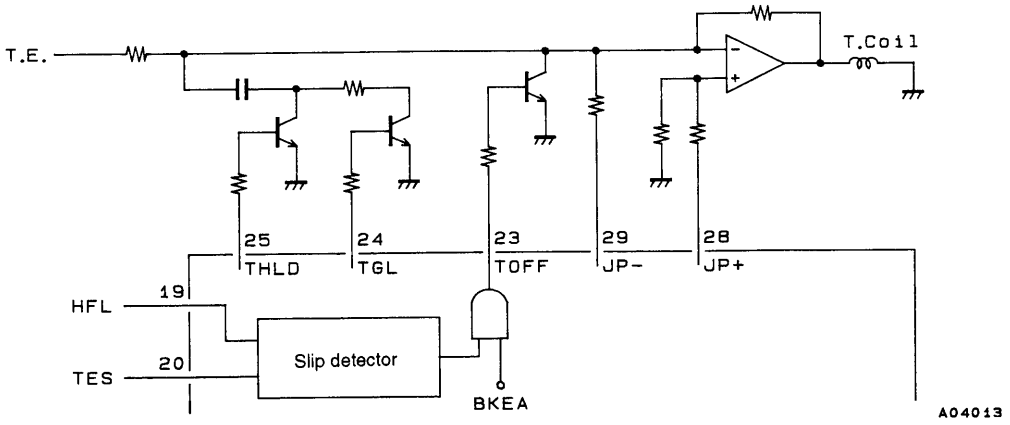
Note: Of the modes related to disk motor control, the TOFF pin only goes low in CLV mode, and will be high during start, stop, and brake operations. Note that the TOFF pin can be turned on and off independently by microprocessor issued commands. However, this function is only valid when disk motor control is in CLV mode.

- Track jump modes

  The table lists the relationships between acceleration pulses (the a period), deceleration pulses (the b period), and the braking period (the c period).

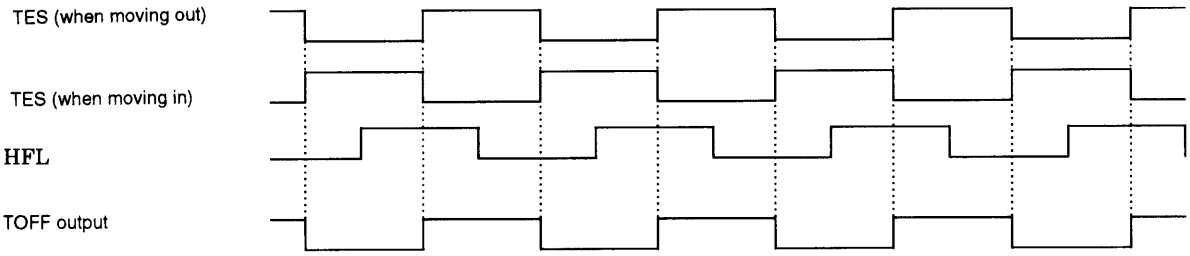
Command	Old track jump mode			New track jump mode		
	a	b	c	a	b	c
1 TRACK JUMP IN (OUT) #1	233 µs	233 µs	60 ms	233 µs	233 µs	60 ms
1 TRACK JUMP IN (OUT) #2	0.5 track jump period	233 µs	60 ms	0.5 track jump period	Same period as a	60 ms
1 TRACK JUMP IN (OUT) #3	0.5 track jump period	233 µs	This period does not exist.	0.5 track jump period	Same period as a	This period does not exist.
1 TRACK JUMP IN (OUT) #4	0.5 track jump period	233 µs	60 ms; TOFF is low during the C period.	0.5 track jump period	Same period as a	60 ms; TOFF is low during the C period.
2 TRACK JUMP IN (OUT)	None	None	None	1 track jump period	Same period as a	This period does not exist.
4 TRACK JUMP IN (OUT)	2 track jump period	466 µs	60 ms	2 track jump period	Same period as a	60 ms
16 TRACK JUMP IN (OUT)	9 track jump period	7 track jump period	60 ms	9 track jump period	Same period as a	60 ms
32 TRACK JUMP IN (OUT)	18 track jump period	14 track jump period	60 ms	18 track jump period	14 track jump period	60 ms
64 TRACK JUMP IN (OUT)	36 track jump period	28 track jump period	60 ms	36 track jump period	28 track jump period	60 ms
128 TRACK JUMP IN (OUT)	72 track jump period	56 track jump period	60 ms	72 track jump period	56 track jump period	60 ms
256 TRACK CHECK	TOFF goes high during the period when 256 tracks are passed over. The a and b pulses are not output.		60 ms	TOFF goes high during the period when 256 tracks are passed over. The a and b pulses are not output.		60 ms
TRACK JUMP BRAKE	There are no a or b periods.		60ms	There are no a and b periods.		60 ms

Note: 1. As indicated in the table, actuator signals are not output during the 256 TRACK CHECK function. This is a mode in which the TES signal is counted in the tracking loop off state. Therefore, feed motor forwarding is required.
2. The servo command register is automatically reset after one cycle of the track jump sequence (a, b, c) completes.
3. A new track jump command cannot be input during a track jump operation.
4. The 1 TRACK JUMP #3 and 2 TRACK JUMP modes do not have a braking period (the c period). Since brake mode must be generated by an external circuit, care is required when using this mode.



When the LC78630E is used in combination with a LA9230/40 Series LSI, since the THLD signal is generated by the LA9230/40 Series LSI, the THLD pin (pin 25) will be unused, i.e., have no connection.

5. Tracking brake
   The chart shows the relationships between the TES, HFL, and TOFF signals during the track jump c period. The TOFF signal is extracted from the HFL signal by TES signal edges. When the HFL signal is high, the pickup is over the mirror surface, and when low, the pickup is over data bits. Thus braking is applied based on the TOFF signal being high when the pickup is moving from a mirror region to a data region and being low when the pickup is moving from a data region to a mirror region.

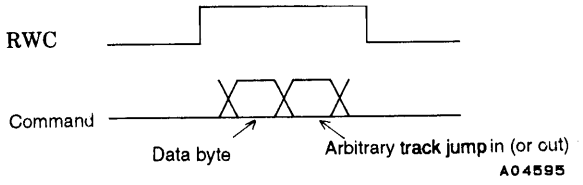


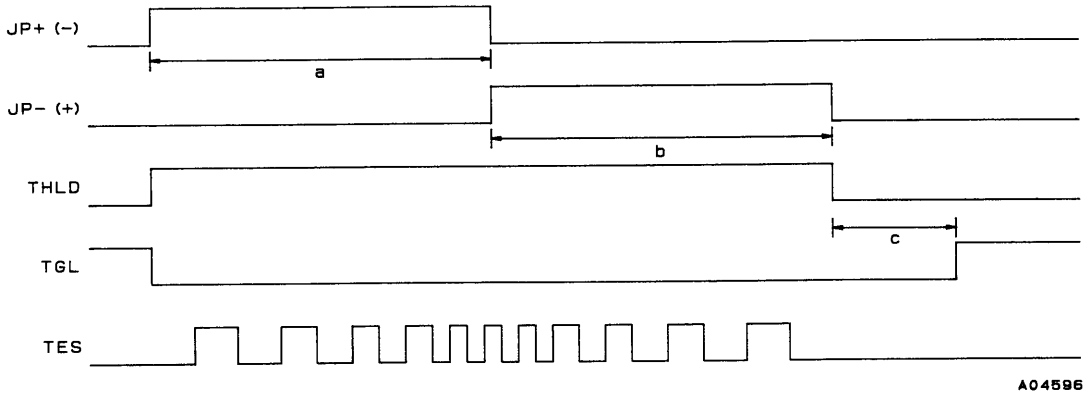
- Arbitrary track jump command

Code	Command	$\overline{\text{RES}}$ = low
$77	ARBITRARY TRACK JUMP IN	
$7F	ARBITRARY TRACK JUMP OUT	
$48	ARBITRARY TRACK JUMP MODE	

The LC78630E performs arbitrary track jump operations specified by an arbitrary binary value in the range 16 to 255 and an arbitrary track jump in or out command. However, to improve pickup set ability, the LC78630E monitors the TES signal half-period, and when it detects a pickup speed of 0, it terminates the track jump operation. Use the old fixed track jump (1TJ and 4TJ) commands to cross 15 or fewer tracks.

DATA BYTE + $77 ($7F)	ARBITRARY TRACK JUMP IN (or OUT)





— Acceleration period (a)
  This period is over when 8/16, 9/16, or 10/16 times the number of tracks to be jumped have been counted. The mode setting command is used to select 8/16, 9/16, or 10/16. The result of this calculation (e.g. (n × 8)/16, where n is the number of tracks to be jumped) is rounded to an integer.

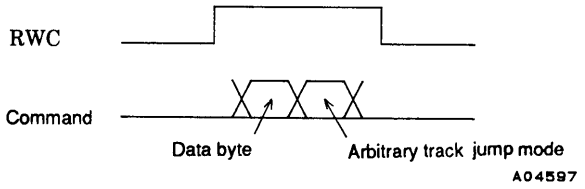
— Deceleration period (b)
  The LC78630E monitors the TES signal half-period, and terminates the operation at the point the set time has passed. The mode setting command is used to set the time. As a b period protection function, the LC78630E terminates the operation if at most the time required for the a period elapses.

— Braking period (c)
This period ends when the WRQ signal rises, i.e. at the point subcodes can be read. If WRQ does not go high, the period is terminated if 60 ms elapse.

Note: Since sled forwarding is not performed, a sled forwarding operation is necessary for large track jumps.

Arbitrary track jump mode is initialized by the following 2-byte command.

DATA BYTE + $48	ARBITRARY TRACK JUMP MODE SET COMMAND



The lower 6 bits of the data byte set the track jump acceleration period (a) and the track jump deceleration period (b). The period a is calculated from the given n and rounded to an integer. The LC78630E monitors the TES half period and terminates the b period if a period longer than the set period elapses.

d5	d4	Track jump acceleration period
0	0	(8/16) × n tracks
0	1	(9/16) × n tracks
1	0	(10/16) × n tracks

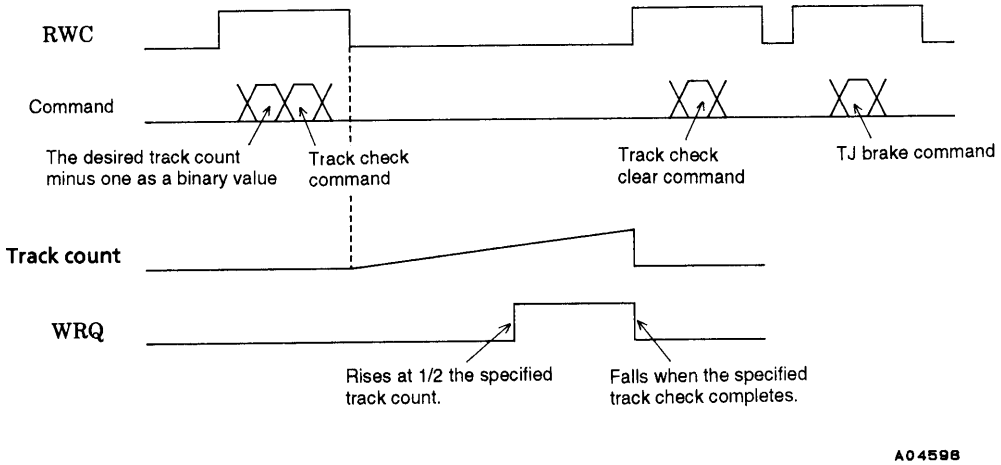
d3	d2	d1	d0	TES half period
0	0	0	0	306 µs*
0	0	0	1	17 µs
0	0	1	0	32 µs
0	1	0	0	62 µs
1	0	0	0	123 µs

The TES half period for b period termination is ≈ (123 × d3) + (62 × d2) + (32 × d1) + (17 × d0) µs
Note: * The maximum value (306 µs) is set when [d3 d2 d1 d0] = [0 0 0 0].

• Track check mode

Code	Command	$\overline{\text{RES}}$ = low
$F0	TRACK CHECK IN	
$F8	TRACK CHECK OUT	
$FF	TRACK CHECK CLEAR	❍

The LC78630E will count the specified number of tracks when the microprocessor sends an arbitrary binary value in the range 8 to 254 and either a track check in or a track check out 2-byte command.



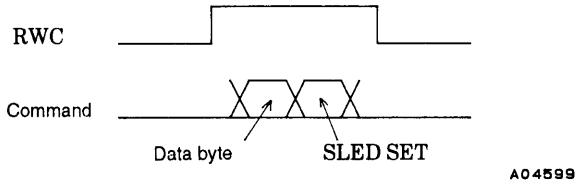
Note: 1. During a track check operation the TOFF pin goes high and the tracking loop is turned off. Therefore, feed motor forwarding is required.
2. When a track check in/out command is issued the function of the WRQ signal switches from the normal mode subcode Q standby monitor function to the track check monitor function. This signal goes high when the track count is half completed, and goes low when the count finishes. The control microprocessor should monitor this signal for a low level to determine when the track check completes.
3. If a track check clear command ($FF) is not issued, the track check operation will repeat. This can be used. For example, to skip over 20,000 tracks, issue a track check 199 code once, and then count the WRQ signal 100 times. This will count 20,000 tracks.
4. After performing a track check operation, use the TJ brake command to lock the pickup onto the track.

7. Sled output; Pin 30: SLD^+, pin 31: SLD^-

Code	Command	$\overline{RES}$ = low
$B8	SLED SET	

The $SLED^+$ and $SLED^-$ outputs can be set independently to one of four levels using this 2-byte command. Neither $SLED^+$ nor $SLED^-$ are output after a reset.

DATA BYTE + $B8	SLED OUTPUT SETTING

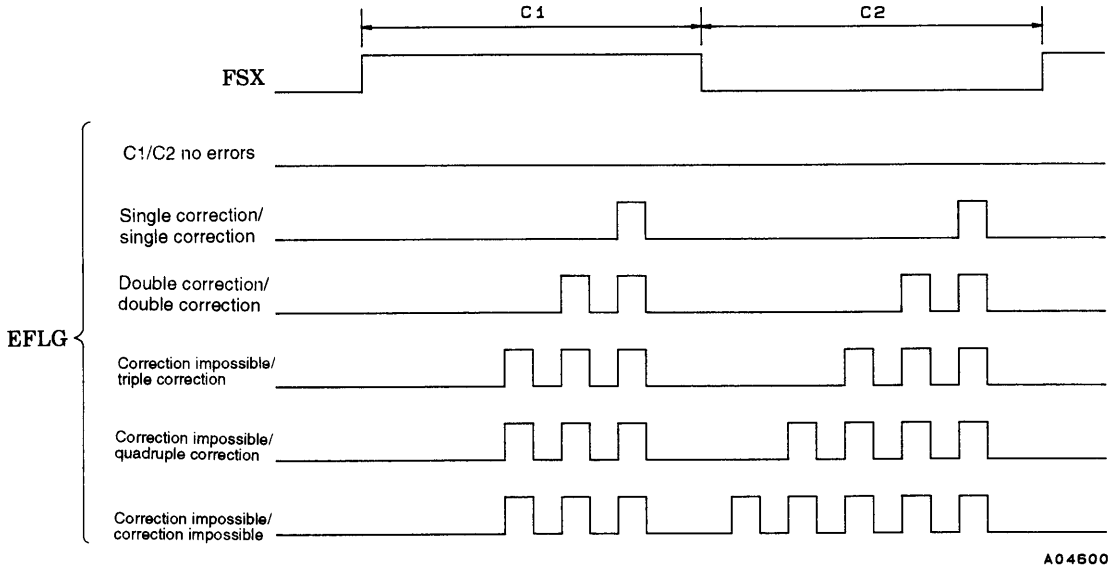


$SLED^+$ and $SLED^-$ output is selected by the most significant bit in the data byte. The SLED output level is set by the lower 3 bits. When $SLED^+$ is set, $SLED^-$ is automatically set to V_{SS} (SLED off). The inverse is also true.

d7	Output pin
0	$SLED^+$
1	$SLED^-$

d2	d1	d0	Output level
0	0	0	V_{SS} (SLED off)
0	0	1	0.25 V_{DD}
0	1	0	0.5 V_{DD}
0	1	1	0.75 V_{DD}
1	0	0	V_{DD}

8. Error flag output; Pin 61: EFLG, pin 66: FSX

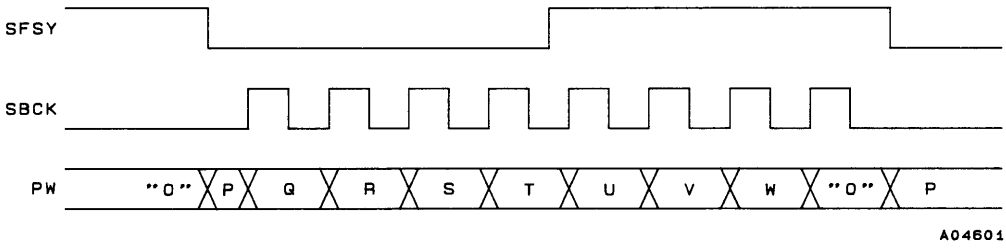


FSX is a 7.35 kHz frame synchronization signal generated by dividing the crystal clock. The error correction state for each frame is output from EFLG. EFLG indicates the C1 correction state while FSX is high and the C2 correction state while FSX is low. The playback OK/NG state can be easily determined from the number of high levels that appear here.

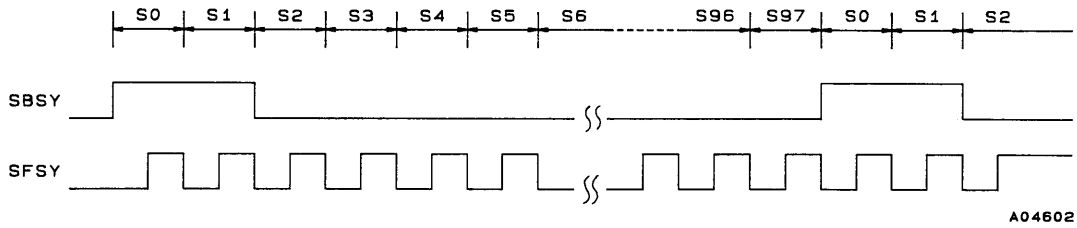
Note: The FSX polarity is opposite in the LC78620 and LC7860 Series LSIs.

9. Subcode P, Q, and R to W output circuit; Pin 62: PW, pin 60: SBSY, pin 63: SFSY, pin 64: SBCK

PW is the subcode signal output pin, and all the codes, P, Q, and R to W can be read out by sending eight clocks to the SBCK pin within 136 µs after the fall of SFSY. The signal that appears on the PW pin changes on the rising edge of SBCK. If a clock is not applied to SBCK, the P code will be output from PW. SFSY is a signal that is output for each subcode frame cycle, and the falling edge of this signal indicates standby for the output of the subcode symbol (P to W). Subcode data P is output on the fall of this signal.



SBSY is a signal output for each subcode block. This signal goes high for the S0 and S1 synchronizing signals. The fall of this signal indicates the end of the subcode synchronizing signals and the start of the data in the subcode block. (EIAJ format)



10. Subcode Q output circuit; Pin 67: WRQ, pin 68: RWC, pin 69: SQOUT, pin 71: CQCK, pin 78: CS

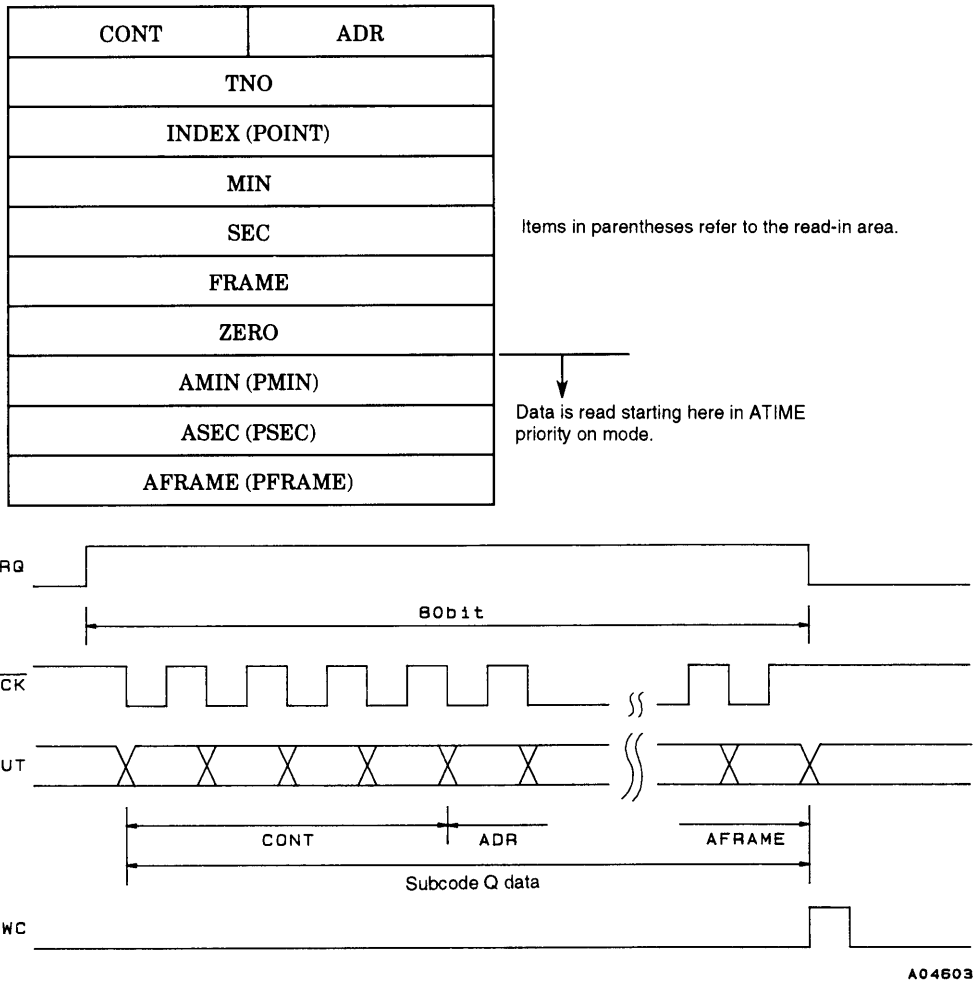
Code	Command	$\overline{\text{RES}}$ = low
$09	ADDRESS FREE	
$89	ADDRESS 1	❍

Subcode Q can be read from the SQOUT pin by applying a clock to the $\overline{\text{CQCK}}$ pin.

Of the eight bits in the subcode, the Q signal is used for song (track) access and display. The WRQ will be high only if the data passed the CRC error check and the subcode Q format internal address is 1*. The control microprocessor can read out data from SQOUT in the order shown below by detecting this high level and applying $\overline{\text{CQCK}}$. When $\overline{\text{CQCK}}$ is applied the DSP disables register update internally. The microprocessor should give update permission by setting RWC high briefly after reading has completed. WRQ will fall to low at this time. Since the WRQ high period is 11.2 ms, $\overline{\text{CQCK}}$ must be applied during the high period. Note that data is read out in an LSB first format.

Note: If RWC is set high by command while WRQ is high, WRQ will return to low and the SQOUT data will be invalid.

Note: * This state will be ignored if an address free command is sent.



Note: 1. Normally, the WRQ pin indicates the subcode Q standby state. However, it is used for a different monitoring purpose in track check mode and during internal braking. (See the items on track checking and internal braking for details.)
2. The LC78630E becomes active when the $\overline{CS}$ pin is low, and subcode Q data is output from the SQOUT pin. When the $\overline{CS}$ pin is high, the SQOUT pin goes to the high-impedance state.

Code	Command	$\overline{RES}$ = low
$4B	ATIME PRIORITY ON	
$4A	ATIME PRIORITY OFF	❍

The ATIME priority command allows the SQOUT output to read from ATIME. In this mode, data is output in a ring sequence in the order: AMIN, ASEC, AFRAME, CONT, ADR, etc.

11. Mute control circuit

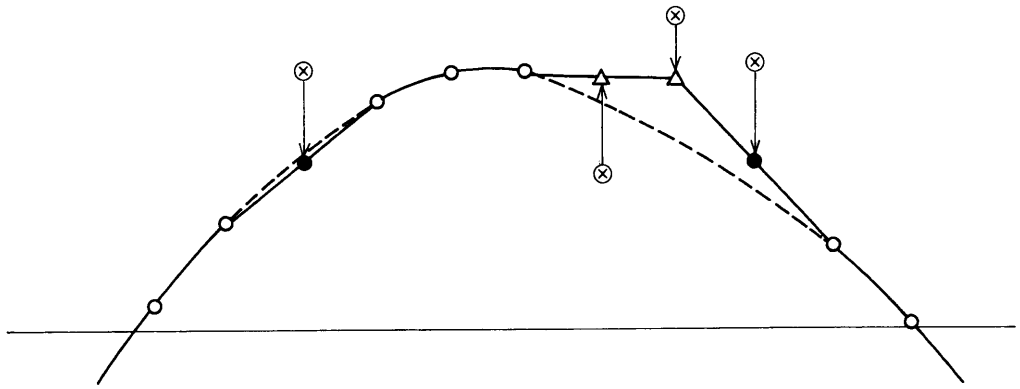
Code	Command	$\overline{RES}$ = low
$01	MUTE 0 dB	
$03	MUTE –∞ dB	❍

Muting of –∞ dB can be applied by issuing the command shown above. The adoption of a zero-cross muting algorithm means that noise is minimal. A zero crossing is recognized when the sign bit of the code changes state.

12. Interpolation circuit

Outputting incorrect audio data that could not be corrected by the error detection and correction circuit would result in loud noises being output. To minimize this noise, the LC78630E replaces incorrect data with linearly interpolated data based on the correct data on both sides of the incorrect data.

If incorrect data continues for two or more consecutive values, the LC78630E holds the previous correct data value and then applies average value interpolation to the previous incorrect value of the next correct data value to calculate the value that precedes the next correct value.



13. Bilingual function

Code	Command	$\overline{RES}$ = low
$28	STO CONT	❍
$29	Lch CONT	
$2A	Rch CONT	

- Following a reset or when a stereo ($28) command has been issued, the left and right channel data is output to the left and right channels respectively.
- When an Lch set ($29) command is issued, the left and right channels both output the left channel data.
- When an Rch set ($2A) command is issued, the left and right channels both output the right channel data.

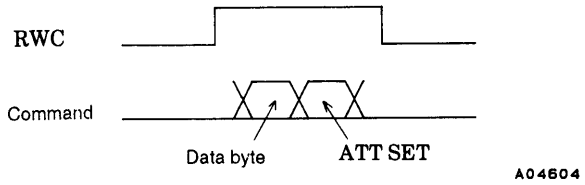
14. De-emphasis; Pin 32: EMPH

The pre-emphasis on/off bit in the subcode Q control information is output from the EMPH pin. When this pin is high, the LC78630E internal de-emphasis circuit operates and the digital filter and the D/A converter output de-emphasized data.

15. Digital attenuator

Attenuation can be applied to the left and right channel audio data independently by issuing two-byte commands. Alternatively, both channels can be attenuated at the same time using the $81 command.

Code	Command	$\overline{RES}$ = low
$81	Lch, Rch ATT SET	
$82	Lch ATT SET	
$83	Rch ATT SET	



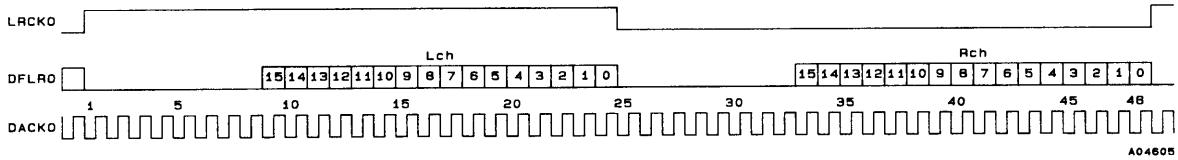
- Attenuation settings
  The attenuation is set by the attenuation data in the first byte and the command in the byte that follows. The data value can be in the range $00 to $EE (0 to 238).

$$\text{Audio output} = 20 \log \frac{\text{ATT DATA}}{256} \text{ [dB]}$$

  — Since the ATT DATA is set to 0 (a muting of –∞) by a reset, to output the audio signal, the control microprocessor must issue, for example, a $EE + $81 command, thus setting both the left and right channels to –0.63 dB.
  Note: To prevent noise due to arithmetic overflow in the 1-bit D/A converter, data values of $EF (ATT DATA = 239) or larger are not allowed.

- Mute output; Pin 46: MUTEL, pin 59: MUTER
  These pins output a high level when the attenuator coefficient is set to $00 and the data in each channel has been zero continuously for a certain period. If data input occurs once again, these pins go low immediately.

16. Digital filter outputs; Pin 34: LRCKO, pin 35: DFLRO, pin 36: DACKO
  DFLRO outputs 2× oversampled data for use with an external D/A converter MSB first in synchronization with the falling edge of DACKO. These pins are provided so that an external D/A converter can be used if desired.

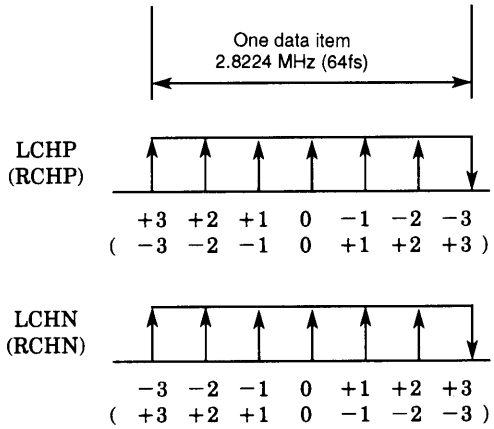


17. Swap; Pin 48: LCHP, pin 49: LCHN, pin 56: RCHN, pin 57: RCHP
  The swap command swaps the D/A converter left and right channel outputs.

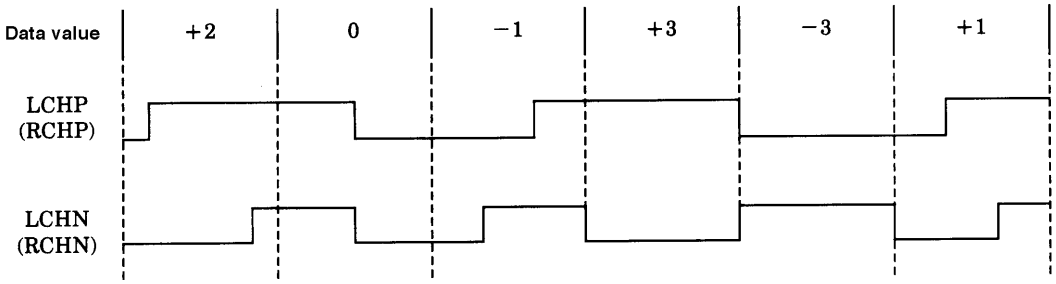
Code	Command	$\overline{\text{RES}}$ = low
$85	SWAP ON	
$84	SWAP OFF	○

18. One-bit D/A converter
  - The LC78630E PWM block outputs one data value in the range –3 to +3 once every 64fs period. To reduce carrier noise, this block adopts an output format in which the output is adjusted so that the PWM output level does not invert between consecutive data items. Also, the attenuator block detects 0 data and enters muting mode so that only a 0 value (a 50% duty signal) is output.
    This block outputs a positive phase signal to the LCHP (RCHP) pin and a negative phase signal to the LCHN (RCHN) pin. High-quality analog signals can be acquired by taking the differences of these two output pairs using external low-pass filters.
    The LC78630E includes built-in radiation suppression resistors (1 kΩ) in each of the LCHP/N and RCHP/N pins.

• PWM output format



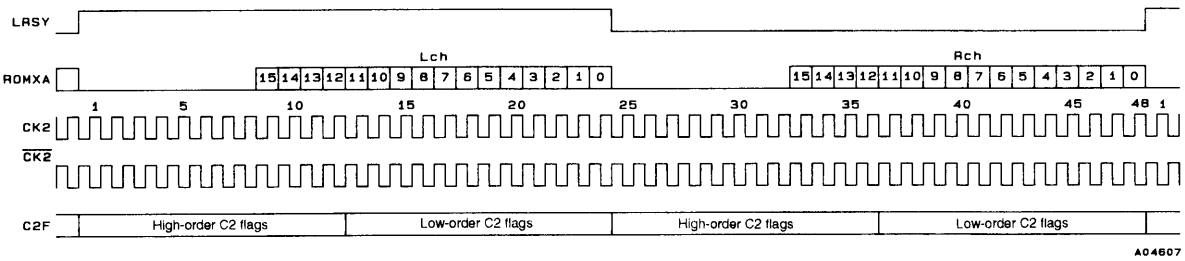
• PWM output example



19. CD-ROM outputs; Pin 42: LRSY, pin 43: CK2, pin 44: ROMXA, pin 45: C2F

Although the LC78630E is initially set up to output audio data MSB first from the ROMXA pin in synchronization with CK2, it can be switched to output CD-ROM data by issuing a CD-ROM XA command. Since this data has not been processed by the interpolation, previous value hold, muting, and other digital circuits, it is appropriate for input to a CD-ROM decoder LSI. CK2 is a 2.1168 MHz clock, and data is output on the CK2 falling edge. However, this clock polarity can be inverted by issuing a CK2 polarity inversion command. C2F is the flag information for the data in 8-bit units. Note that the CD-ROM XA reset command has the same function as the CONT1 pin (pin 37).

Code	Command	$\overline{\text{RES}}$ = low
$88	CD ROM XA	
$8B	CONT AND CD-ROM XA RESET	❍
$C9	CK2 POLARITY INVERSION	



20. Digital output circuit; Pin 65: DOUT
    This is an output pin for use with a digital audio interface. Data is output in the EIAJ format. This signal has been processed by the interpolation and muting circuits. This pin has a built-in driver circuit and can directly drive a transformer.

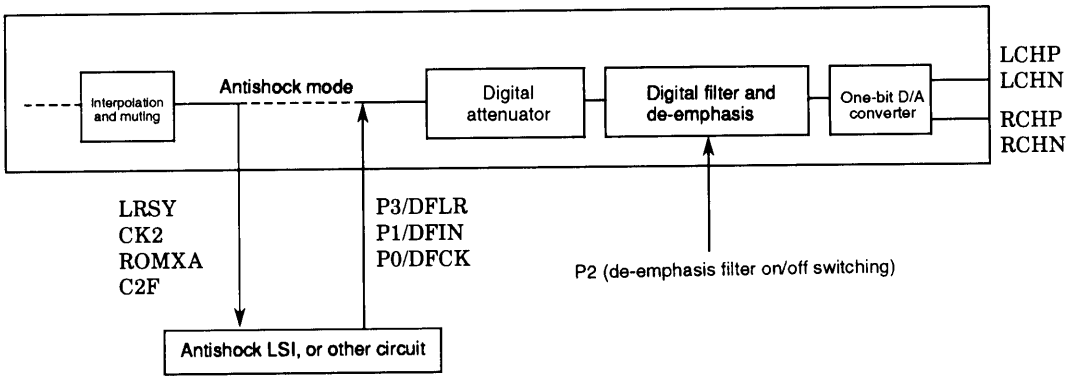
Code	Command	$\overline{RES}$ = low
$42	DOUT ON	❍
$43	DOUT OFF	
$40	UBIT ON	❍
$41	UBIT OFF	

- The digital OUT pin can be locked at the low level by issuing a DOUT OFF command.
- The UBIT information in the DOUT data can be locked at zero by issuing a UBIT OFF command.
- The DOUT data can be switched to data to which interpolation and muting have not been applied by issuing a CD-ROM XA command.

21. Antishock support; Pin 38: P0/DFCK, pin 39: P1/DFIN, pin 40: P2, pin 41: P3/DFLR, pin 42: LRSY, pin 43: CK2, pin 44: ROMXA, pin 45: C2F
    Antishock mode is a mode in which antishock processing is applied to data that has been output once. That data is returned and output once again as an audio playback signal. It is also possible to use only the audio playback block (the attenuator, digital filter, and D/A converter circuits) and thus share the audio playback block with other systems by synchronizing the other system with the LC78630E clock.

Code	Command	$\overline{RES}$ = low
$6C	ANTI-SHOCK ON	
$6B	ANTI-SHOCK OFF	❍
$6F	DF NORMAL SPEED ON (only in antishock mode)	
$6E	DF NORMAL SPEED OFF (only in antishock mode)	❍

- The signals from the ROMXA pin can be output to an antishock LSI (the Sanyo LC89151) and re-input the signals output by the antishock LSI to the LC78630E P1/DFIN pin. These signals are then processed by the attenuator, digital filters, and D/A converter circuits and output as audio signals. In this mode, the P2 pin switches the de-emphasis filter on and off. When P2 is high, the de-emphasis filter will be on.
- In antishock systems, the signal-processing block must operate in double-speed playback mode for data output to the antishock LSI, and the audio playback block (the attenuator, digital filter, and D/A converter circuits) must operate at normal speed. This means that the control microprocessor must issue both the antishock on command ($6C) as well as the DF normal speed on command ($6F).



22. General-purpose output ports; Pin 37: CONT1, pin 74: CONT2
The CONT1 and CONT2 pins can be set to high or low by commands from the control microprocessor.

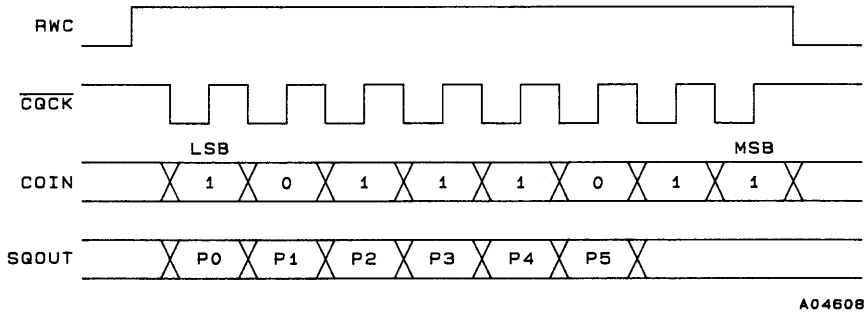
Code	Command	$\overline{RES}$ = low
$0E	CONT1 SET	
$8B	CONT1 AND CD-ROM XA RESET	❍
$4D	CONT2 SET	
$4C	CONT2 RESET	❍

Note that the CONT1 reset command also resets the CD-ROM XA mode, and thus care is required when using this command.

23. General-purpose I/O ports; Pin 38: P0/DFCK, pin 39: P1/DFIN, pin 40: P2, pin 41: P3/DFLR, pin 18: P4, pin 33: P5
The LC78630E provide six I/O ports: pins P0 to P5. These pins all function as input pins after a reset. Unused ports must be connected to ground or set to output mode.

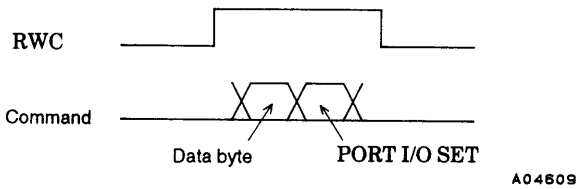
Code	Command	$\overline{RES}$ = low
$DD	PORT READ	
$DB	PORT I/O SET	
$DC	PORT OUTPUT	

The port information can be read from the SQOUT pin in the order P0 to P5 in synchronization with $\overline{CQCK}$ falling edges by issuing the port read command. Note that data can be read out in the same manner when another command is issued.



These ports can be set independently to be control output pins by the two-byte port I/O set command. Ports are selected with the lower 6 bits of the data byte.

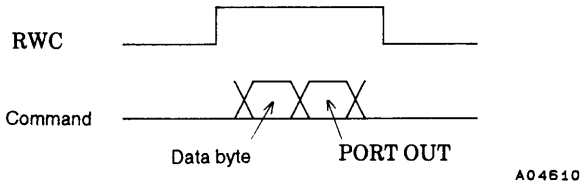
DATA BYTE + $DB	PORT I/O SET



dn = 1 .....Sets port Pn to be an output pin.
dn = 0 .....Sets port Pn to be an input pin.
n = 0 to 5

Ports set to be output pins can be independently set to be either high or low by the port output two-byte command. The lower 6 bits of the data byte correspond to the ports.

DATA BYTE + $DC	PORT OUTPUT



dn = 1 .....A high level is output from Pn, assuming it is set up for output.
dn = 0 .....A low level is output from Pn, assuming it is set up for output.

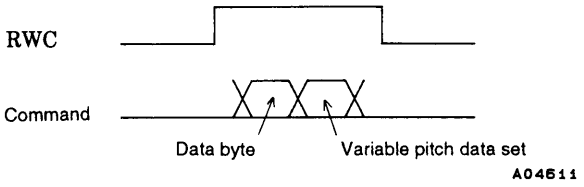
24. Variable pitch playback; Pin 1: VPDO, pin 80 VCOC

The LC78630E includes a variable pitch PLL circuit, and the disk rotation rate and the ROMXA output data transfer rate can be varied by varying the clock used as the time base in 0.1% increments over a range of ±13%. A variable pitch circuit is formed by connecting a variable pitch low-pass filter to the VPDO and VCOC pins.
Note: Variable pitch playback is not supported at 4× speed.

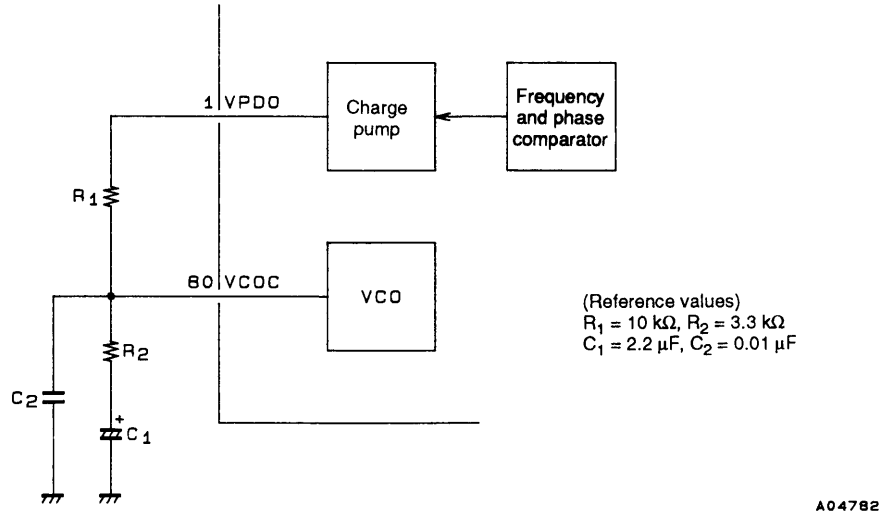
Code	Command	$\overline{RES}$ = low
$D9	VARIABLE PITCH ON	
$D8	VARIABLE PITCH OFF	❍
$DA	VARIABLE PITCH DATA SET	

The amount of variation is set by the data byte value n (as a two's complement number) and the variable pitch data set two-byte command.

DATA BYTE + $DA	VARIABLE PITCH DATA SET



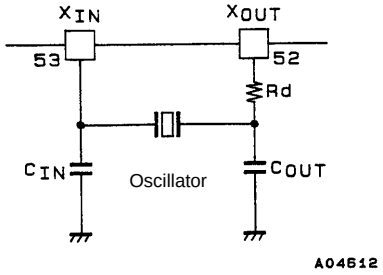
Amount of change = n/10 [%] (n = –128 to +127)



25. Clock oscillator; Pin 53: X_{IN}, pin 52: X_{OUT}

Code	Command	$\overline{RES}$ = low
$8E	OSC ON	❍
$8D	OSC OFF	
$CE	XTAL 16M	❍
$CF	XTAL 32M	
$C2	NORMAL-SPEED PLAYBACK	❍
$C1	DOUBLE-SPEED PLAYBACK	
$C8	QUAD-SPEED PLAYBACK	

The clock that is used as the time base is generated by connecting a 16.9344 or 33.8688 MHz oscillator element between these pins. The OSC OFF command turns off both the VCO and crystal oscillators. Double- or quad-speed playback can be specified by microprocessor command.



- Use a 16.9344 MHz oscillator element if the application circuit implements a 2×-speed playback system. The system control microprocessor can then issue 2×-speed or normal-speed playback commands.
- Use a 33.8688 MHz oscillator element if the application circuit implements a 4×-speed playback system. The system control microprocessor can then issue 4×-speed, 2×-speed, or normal-speed playback commands.

26. 16M and 4.2M pins; Pin 75: 16M, pin 76: 4.2M

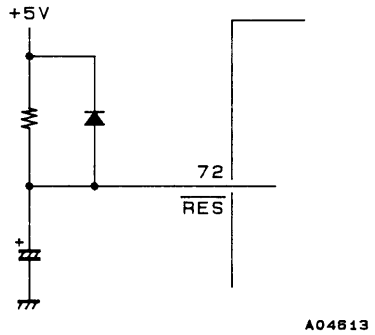
If a 16.9344 MHz oscillator element is used, the 16M pin will output a 16.9344 MHz signal from a buffer circuit in 2×-speed and normal-speed playback modes. If a 33.8688 MHz oscillator element is used, the 16M pin will output a 33.8688 MHz signal from a buffer circuit in 4×-speed playback mode. The 4.2M pin functions as the LA9230/LA9240 Series system clocks and always outputs a 4.2336 MHz signal. In oscillator off mode, both of these pins are held either high or low.

27. Reset circuit: Pin 72: $\overline{RES}$

This pin must be pulled low temporarily and then set high after power is first applied. This sets the muting to –∞ dB and the disc motor to stopped.

CLV servo system	START	[STOP]	BRAKE	CLV
Muting control	0 dB	[–∞]		
Subcode Q address conditions	[Address 1]	Address free		
CONT1, CONT2	High	[Low]		
Track jump mode	[Old]	New		
Track count mode	Old	[New]		
Digital attenuator	[DATA $00]	DATA $00 to $EE		
OSC	[ON]	OFF		
XTAL	[16M]	32M		
Playback speed	[Normal speed]	Double speed	Quad speed	
Antishock mode	ON	[OFF]		
General-purpose input ports	[All pins input]	Input or output set independently		
Digital filter normal speed	ON	[OFF]		

Setting the $\overline{RES}$ pin low directly sets the states enclosed in boxes.



28. Other pins; Pin 8: TAI, pin 12: TEST1, pin 16: TEST2, pin 17: TEST3, pin 26: TEST4, pin 77: TEST5, pin 73: TESTF

    These are test pins for testing the LSI internal circuits. TAI and TEST1 to TEST5 have built-in pull-down resistors.

29. RAM address control

    The LC78630E incorporates an 8-bit × 2336-word RAM on chip. This RAM provides an EFM demodulated data jitter handling capacity of ±8 frames implemented using address control. The LC78630E continuously checks the remaining buffer capacity and controls the data write address to fall in the center of the buffer capacity by making fine adjustments to the frequency divisor in the PCK side of the CLV servo circuit. If the ±8 frame buffer capacity is exceeded, the LC78630E forcibly sets the write address to the ±0 position. However, since the errors that occur due to this operation cannot be handled with error flag processing, the IC applies muting to the output for a 109 frame period.

Position	Division ratio or processing
–8 or lower	Forcibly moves to ±0
–7 to –1	Advancing divisor: 589
±0	Standard divisor: 588
+1 to +7	Fall back divisor: 587
+8 or greater	Forcibly moves to ±0

Command Table

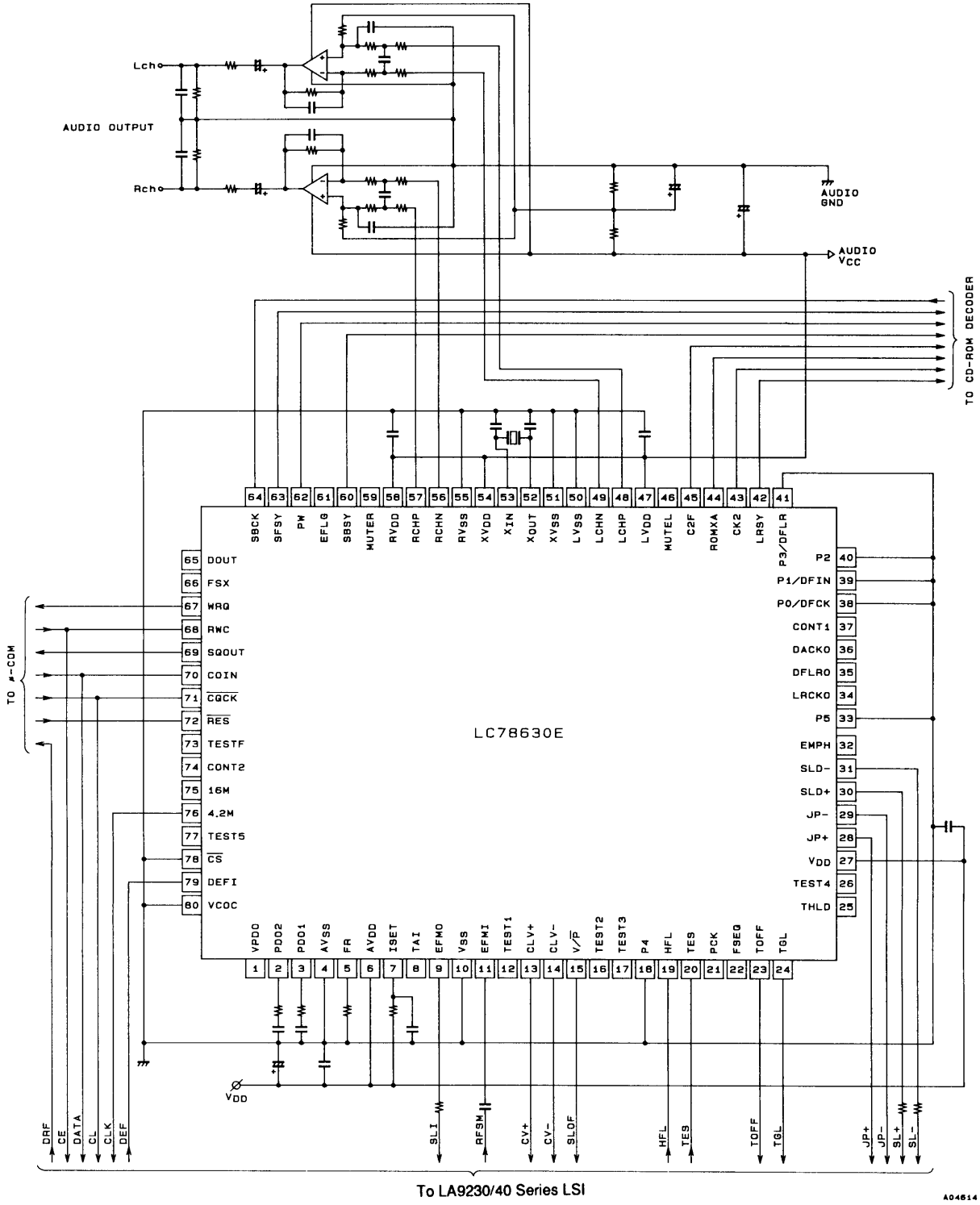
Blank entries: Unused command
Items in parentheses as ASP commands
All commands, except the TJ BRAKE ($8C), NOTHING ($FE), and TCHK CLEAR ($FF) are latched.

$00	(ADJ. RESET)	$20	THLD PERIOD TOFF LOW	$40	UBIT ON	$60	
$01	MUTE 0 dB	$21	THLD PERIOD TOFF HIGH	$41	UBIT OFF	$61	
$02		$22	NEW TRACK CNT	$42	DOUT ON	$62	
$03	MUTE –∞ dB	$23	OLD TRACK CNT	$43	DOUT OFF	$63	
$04	DM START	$24		$44		$64	
$05	DM CLV	$25		$45		$65	
$06	DM BRAKE	$26		$46		$66	
$07	DM STOP	$27		$47		$67	
$08		$28	STO CONT	$48	NTJ COND SET	$68	
$09	ADDRESS FREE	$29	LCH CONT	$49	PCK OFF	$69	
$0A		$2A	RCH CONT	$4A	ATIME PRIORITY OFF	$6A	
$0B		$2B		$4B	ATIME PRIORITY ON	$6B	ANTI-SHOCK OFF
$0C		$2C		$4C	CONT2 RST	$6C	ANTI-SHOCK ON
$0D		$2D		$4D	CONT2 SET	$6D	
$0E	CONT1 SET	$2E		$4E		$6E	DF NORMAL SPEED OFF
$0F	TRACKING OFF	$2F		$4F		$6F	DF NORMAL SPEED ON
$10	2TJ IN	$30	32TJ IN	$50		$70	
$11	1TJ IN #1	$31	1TJ IN #3	$51		$71	
$12	1TJ IN #2	$32		$52	1TJ IN #4	$72	
$13	4TJ IN	$33		$53		$73	
$14	16TJ IN	$34		$54		$74	
$15	64TJ IN	$35		$55		$75	
$16	256TCHK	$36		$56		$76	
$17	128TJ IN	$37		$57		$77	NTJ IN
$18	2TJ OUT	$38	32TJ OUT	$58		$78	
$19	1TJ OUT #1	$39	1TJ OUT #3	$59		$79	
$1A	1TJ OUT #2	$3A		$5A	1TJ OUT #4	$7A	
$1B	4TJ OUT	$3B		$5B		$7B	
$1C	16TJ OUT	$3C		$5C		$7C	
$1D	64TJ OUT	$3D		$5D		$7D	
$1E		$3E		$5E		$7E	
$1F	128TJ OUT	$3F		$5F		$7F	NTJ OUT

Blank entries: Unused command
Items in parentheses as ASP commands
All commands, except the TJ BRAKE ($8C), NOTHING ($FE), and TCHK CLEAR ($FF) are latched.

$80		$A0	OLD TRACK JUMP	$C0		$E0	
$81	LRCH ATT SET	$A1	NEW TRACK JUMP	$C1	DOUBLE-SPEED PLAYBACK	$E1	
$82	LCH ATT SET	$A2		$C2	NORMAL-SPEED PLAYBACK	$E2	
$83	RCH ATT SET	$A3	INTERNAL BRAKE CONT	$C3		$E3	
$84	SWAP OFF	$A4		$C4	INTERNAL BRAKE OFF	$E4	
$85	SWAP ON	$A5		$C5	INTERNAL BRAKE ON	$E5	
$86		$A6		$C6		$E6	
$87		$A7		$C7		$E7	
$88	CDROMXA	$A8	DISK 8cm SET	$C8	QUAD-SPEED PLAYBACK	$E8	
$89	ADDRESS1	$A9	DISK 12cm SET	$C9	CK2 POLARITY INVERSION	$E9	
$8A		$AA		$CA	INTERNAL BRAKE CONTINUOUS OFF	$EA	
$8B	CNT1, ROMXA RST	$AB		$CB	INTERNAL BRAKE CONTINUOUS ON	$EB	
$8C	TJ BRAKE	$AC		$CC	INTERNAL BRAKE TRKG OFF	$EC	
$8D	OSC OFF	$AD		$CD	INTERNAL BRAKE TRKG ON	$ED	
$8E	OSC ON	$AE		$CE	XTAL 16M	$EE	COMMAND NOISE REDUCTION MODE OFF
$8F	TRACKING ON	$AF		$CF	XTAL 32M	$EF	COMMAND NOISE REDUCTION MODE ON
$90	(F.OFS. ADJ. ST)	$B0	NO CLV PHASE COMPARATOR DIVISOR	$D0		$F0	TRACK CHK IN
$91	(F.OFS. ADJ. OFF)	$B1	CLV PHASE COMPARATOR DIVISOR: 1/2	$D1		$F1	
$92	(T.OFS. ADJ. ST)	$B2	CLV PHASE COMPARATOR DIVISOR: 1/4	$D2		$F2	
$93	(T.OFS. ADJ. OFF)	$B3	CLV PHASE COMPARATOR DIVISOR: 1/8	$D3		$F3	
$94	(LSR. ON)	$B4		$D4		$F4	
$95	(LSR. OFF/F. SV. ON)	$B5		$D5		$F5	
$96	(LSR. OFF/F. SV. OFF)	$B6		$D6		$F6	
$97	(SP. 8CM)	$B7		$D7		$F7	
$98	(SP. 12CM)	$B8	SLED SET	$D8	VARIABLE PITCH OFF	$F8	TRACK CHK OUT
$99	(SP. OFF)	$B9		$D9	VARIABLE PITCH ON	$F9	
$9A	(SLED. ON)	$BA	TES WD WIDE	$DA	VARIABLE PITCH SET	$FA	
$9B	(SLED. OFF)	$BB	TES WD NARW	$DB	PORT I/O SET	$FB	
$9C	(EF. BAL. ST)	$BC		$DC	PORT OUTPUT	$FC	
$9D	(T. SV. OFF)	$BD		$DD	PORT READ	$FD	
$9E	(T. SV. ON)	$BE		$DE		$FE	NOTHING
$9F		$BF		$DF		$FF	TCHK CLEAR

Sample Application Circuit



Item		LC7861NE → LC7861KE	LC78621E	LC78622E	LC78624E	LC78625E	LC78626E	LC78630E
EFMPLL		Paired with LA9210M	Built-in VCO FR = 1.2 kΩ	Built-in VCO FR = 1.2 kΩ	Built-in VCO FR = 1.2 kΩ	Built-in VCO FR = 1.2 kΩ	Built-in VCO FR = 5.1 kΩ	Built-in VCO FR = 1.2 kΩ
RAM		16K	16K	16K	16K	16K	16K	18k
Playback speed		2× (4×)	2×	2×	2×	2×	2×	4×
Digital output		❍	❍	❍	❍	❍	❍	❍
Interpolation		4	4	2	2	4	2	2
Zero-cross muting		❍ –12 dB, –∞	❍ –12 dB, –∞	❍ –∞	❍ –∞	❍ –12 dB, –∞	❍ –∞	❍ –∞
Level meter & peak search		×	❍	×	×	❍	×	×
Bilingual		×	❍	❍	❍	❍	❍	❍
Digital attenuator		×	❍	❍	×	❍	❍	❍
Digital filters		2fs	8fs	4fs	×	8fs	4fs	2fs
Digital de-emphasis		×	❍	❍	×	❍	❍	❍
General-purpose ports	Output	2	2	×	×	2	×	2
	I/O	×	×	5	5	(4)	1 + (3)	2 + (4)
Video CD support		×	×	×	×	❍	×	❍
Anti-shock interface		×	❍	×	×	❍	Unnecessary	❍
Anti-shock controller		×	×	×	×	×	❍	×
CD text		×	×	×	❍	×	×	×
CD-ROM interface		❍	❍	×	×	❍	×	❍
1 bit D/A converter		×	❍	❍	×	❍	❍	❍
Low pass filter		×	×	❍	×	×	❍	×
Supply voltage		4.5 to 5.5 V	3.6 to 5.5 V	3.0 to 5.5 V	3.0 to 5.5 V	3.0 to 5.5 V	3.0 to 5.5 V	3.6 to 5.5 V
Package		QFP64E	QFP80E	QFP64E	QFP64E	QFP80E	QFP100E	QFP80E

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